

**SANYO****Character and Pattern Display Control IC****Overview**

Character and pattern display control IC for TV screen. A character dot configuration is  $12 \times 18$ . The IC has 64 internal character ROMs and displays up to 288 characters (24 characters  $\times$  12 lines) on a TV screen. It can be controlled by a microcontroller.

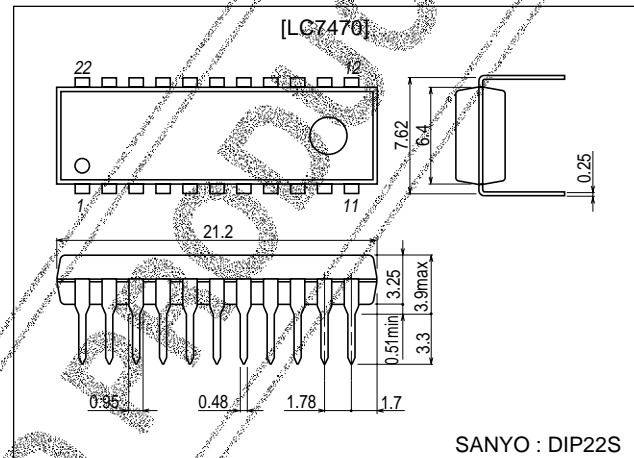
**Function and Applications**

- Screen Display Mode: 24 characters  $\times$  12 lines
- Number of display characters: 288 characters (max.)
- Display control ROM (line ROM):
  - 64 lines (line control: 24-character line)
- Display RAM:
  - 176 characters (used for specifying variable characters)
- Character configuration:
  - 12 (horizontal)  $\times$  18 (vertical) dots
- Number of character types: 64 types
- Character size:
  - Horizontal direction: 4, Vertical direction: 4
- Display start position:
  - Horizontal direction: 64, Vertical direction: 64
- Blinking mode: Character blinking
- Display ON/OFF mode:
  - ON/OFF cycle; 1.0 second and 0.5 second. Duty cycle: 25%, 50% and 75%
- Blanking mode: Entire font area ( $12 \times 18$  dots)
- Background colors: 4 (at internal SYNC operation mode)
- External control input: Serial data input
- Synchronous signal: Selectable: Internal and External
- Internal SYNC. separation circuit available.
- Video output: NTSC-format composite output
- Superimpose function:
  - Superimposes character output on composite video output

**Package Dimensions**

unit:mm

3059-DIP22S



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**SANYO Electric Co.,Ltd. Semiconductor Company**

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

# LC7470

## Specifications

### Absolute Maximum Ratings

Parameter	Symbol	Condition	Ratings	Unit
Maximum supply voltage	$V_{DD}$	$V_{DD1}, V_{DD2}$	$V_{SS}-0.3$ to $V_{SS}+7.0$	V
Maximum input voltage	$V_{IN}$	All input pins	$V_{SS}-0.3$ to $V_{DD1}+0.3$	V
Maximum output voltage	$V_{OUT}$		$V_{SS}-0.3$ to $V_{DD1}+0.3$	V
Allowable power dissipation	$Pd$ max	$T_a = 25^\circ C$	300	mW
Operating temperature	$T_{opr}$		-30 to +70	$^\circ C$
Storage temperature	$T_{stg}$		-40 to +125	$^\circ C$

### Recommended Operating Conditions at $T_a = -30$ to $+70^\circ C$

Parameter	Symbol	Condition	Ratings			Unit
			min	typ	max	
Supply voltage	$V_{DD1}$	Pin $V_{DD1}$	4.5	5.0	5.5	V
	$V_{DD2}$	Pin $V_{DD2}$	4.5	5.0	$1.27V_{DD1}$	V
Input high-level voltage	$V_{IH2}$	Pins $\overline{CS}$ , SIN, RST, SCLK	$0.8V_{DD1}$		$V_{DD1}+0.3$	V
Input low-level voltage	$V_{IL2}$	Pins $\overline{CS}$ , SIN, RST, SCLK	$V_{SS}-0.3$		$0.2V_{DD1}$	V
Composite video input voltage	$V_{IN1}$	$CV_{IN}$		2Vp-p		V
	$V_{IN2}$	Pin SYNI		2Vp-p	2.5Vp-p	
Oscillation frequency	FOSC1	Xtal oscillation pin (at $4f_{OSC}$ )		14.31		MHz
	FOSC2	Xtal oscillation pin (at $2f_{OSC}$ )		7.16		MHz
	FOSC3	LC oscillation pin		7		MHz

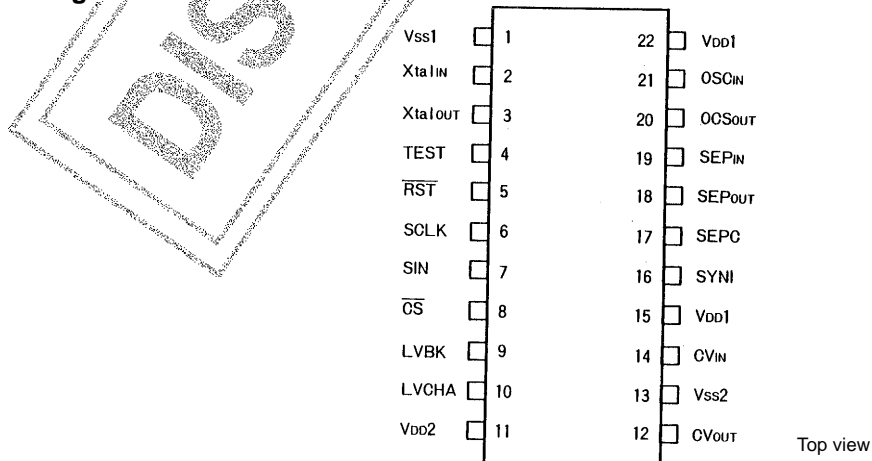
### Electrical Characteristics at $T_a = -30$ C to $+70^\circ C$ , and $V_{DD} = 5V$ unless other noted

Parameter	Symbol	Condition	Ratings			Unit
			min	typ	max	
Output-off leakage current	$I_{leak}$	$CV_{OUT}$			10	$\mu A$
Output high-level voltage	$V_{IH1}$	SEP <sub>OUT</sub> , $V_{DD}=4.5V$ , $I_{OH}=1.0mA$	3.5			V
Output low-level voltage	$V_{IL1}$	SEP <sub>OUT</sub> , $V_{DD}=4.5V$ , $I_{OL}=1.0mA$			1.0	V
Input current	$I_{IH}$	$\overline{CS}$ , SIN, RST, SCLK, SEP <sub>IN</sub> , $V_{IN}=V_{DD}$			1	$\mu A$
	$I_{IL}$	OSC <sub>IN</sub> , $V_{IN}=V_{SS}$	-1			$\mu A$
Operating current drain	$I_{DD}$				15	mA

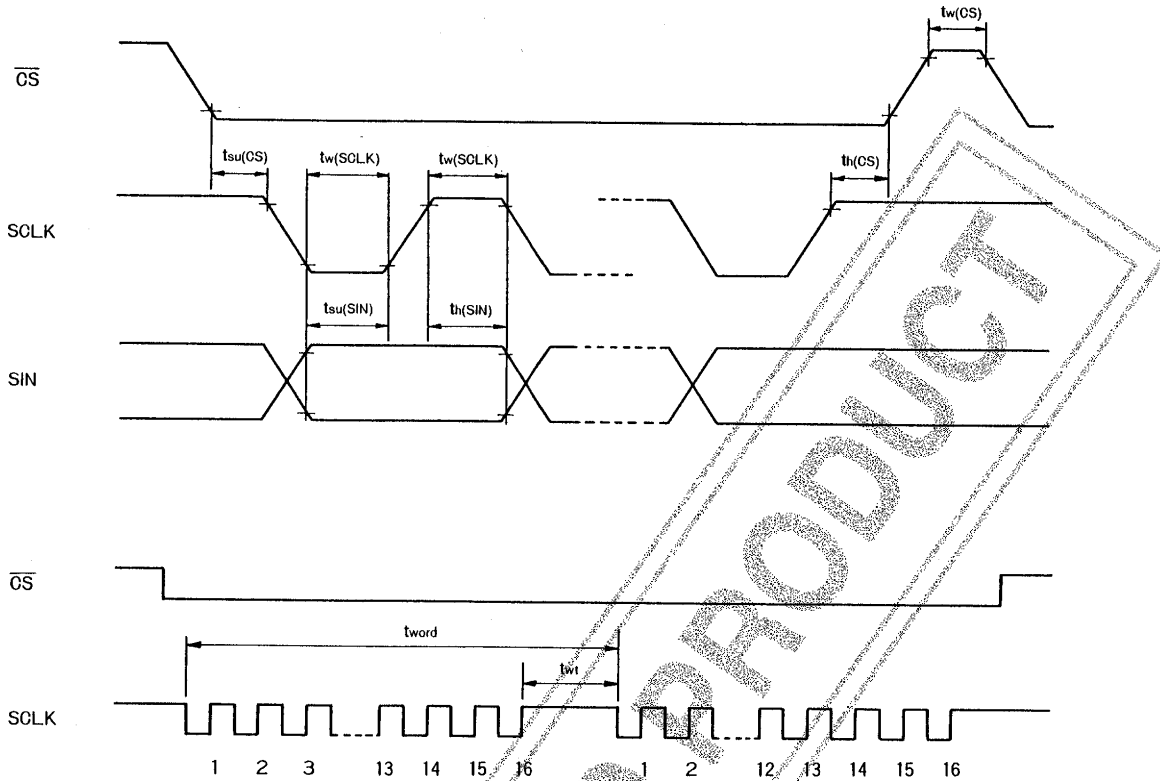
### Timing Characteristics at $T_a = -30$ to $+70^\circ C$ , $V_{DD} = 5 \pm 0.5V$

Parameter	Symbol	Condition	Ratings			Unit
			min	typ	max	
Minimum input pulse width	$t_w(SCLK)$	SCLK	200			ns
	$t_w(\overline{CS})$	$\overline{CS}$ ( $\overline{CS}$ =H-level period)	1			$\mu s$
Data setup time	$t_{su}(\overline{CS})$	$\overline{CS}$	200			ns
	$t_{su}(SIN)$	SIN	200			ns
Data hold time	$t_h(\overline{CS})$	$\overline{CS}$		2		$\mu s$
	$t_h(SIN)$	SIN		200		ns
1-word write period	$t_{word}$	16-bit data write period	10			$\mu s$
	$t_{wt}$	RAM data write period	1			$\mu s$

### Pin Assignment



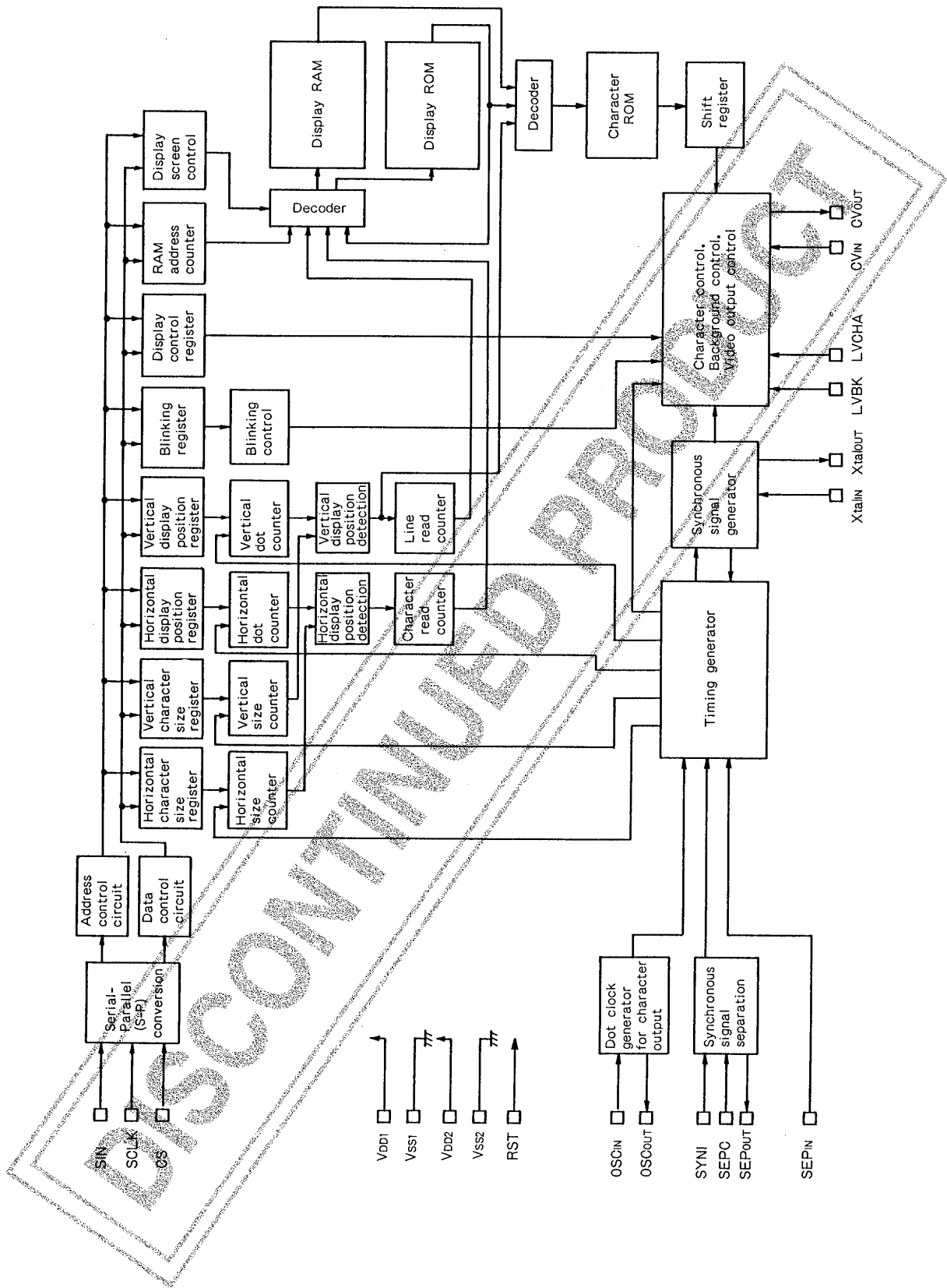
Serial Data Input Timings



Pin Description

Pin No.	Pin symbol	Pin Name	Functions
1	V <sub>SS1</sub>	Ground pin	GND pin (digital grounding)
2	Xtal <sub>IN</sub>	Xtal oscillation pin	Oscillation pins for connecting a crystal oscillator and capacitor to generate internal synchronous signals
3	Xtal <sub>OUT</sub>		
4	TEST	Test pin	Test output pin
5	RST	Reset input pin	System reset input pin
6	SCLK	Clock input pin	Clock input pin for serial data input
7	SIN	Data input pin	Serial data input pin. Serial 16-bit data input is supported
8	CS	Enable input pin	Enable input pin for serial data input. If this pin becomes active (active low), the serial data input is enabled
9	LVBK	Input pin for blank level adjustment	Level input pin for adjusting blank levels
10	LVCHA	Input pin for character level adjustment	Level input pin for adjusting character levels
11	V <sub>DD2</sub>	Power supply pin	Power supply pin for adjusting composite video signal levels (analog power supply)
12	CV <sub>OUT</sub>	Video signal output pin	Output pin for composite video signal
13	V <sub>SS2</sub>	Ground pin	GND pin (analog grounding)
14	CV <sub>IN</sub>	Video signal input pin	Input pin for composite video signal
15	V <sub>DD1</sub>	Supply voltage pin	Supply voltage pin (+5V)
16	SYN <sub>I</sub>	Synchronous signal separation circuit input pin	Input pin for synchronous signal separation circuit
17	SEPC	Synchronous signal separation circuit adjustment pin	Adjustment pin for synchronous signal separation circuit (A capacitor is connected to this pin)
18	SEPOUT	Composite synchronous signal output pin	Composite synchronous signal output pin for synchronous signal separation circuit
19	SEPIN	Vertical synchronous signal input pin	Vertical synchronous signal input pin. The input signal to this pin is generated by integrating the output signal from the SEPOUT pin. Add an integral circuit between the SEPOUT pin and the SEPIN pin
20	OSC <sub>OUT</sub>	LC oscillation pin	Oscillation pins for connecting a coil and capacitor to generate character output dot clocks
21	OSC <sub>IN</sub>		
22	V <sub>DD1</sub>	Supply voltage pin (+5V)	Supply voltage (+5V)

System Block Diagram

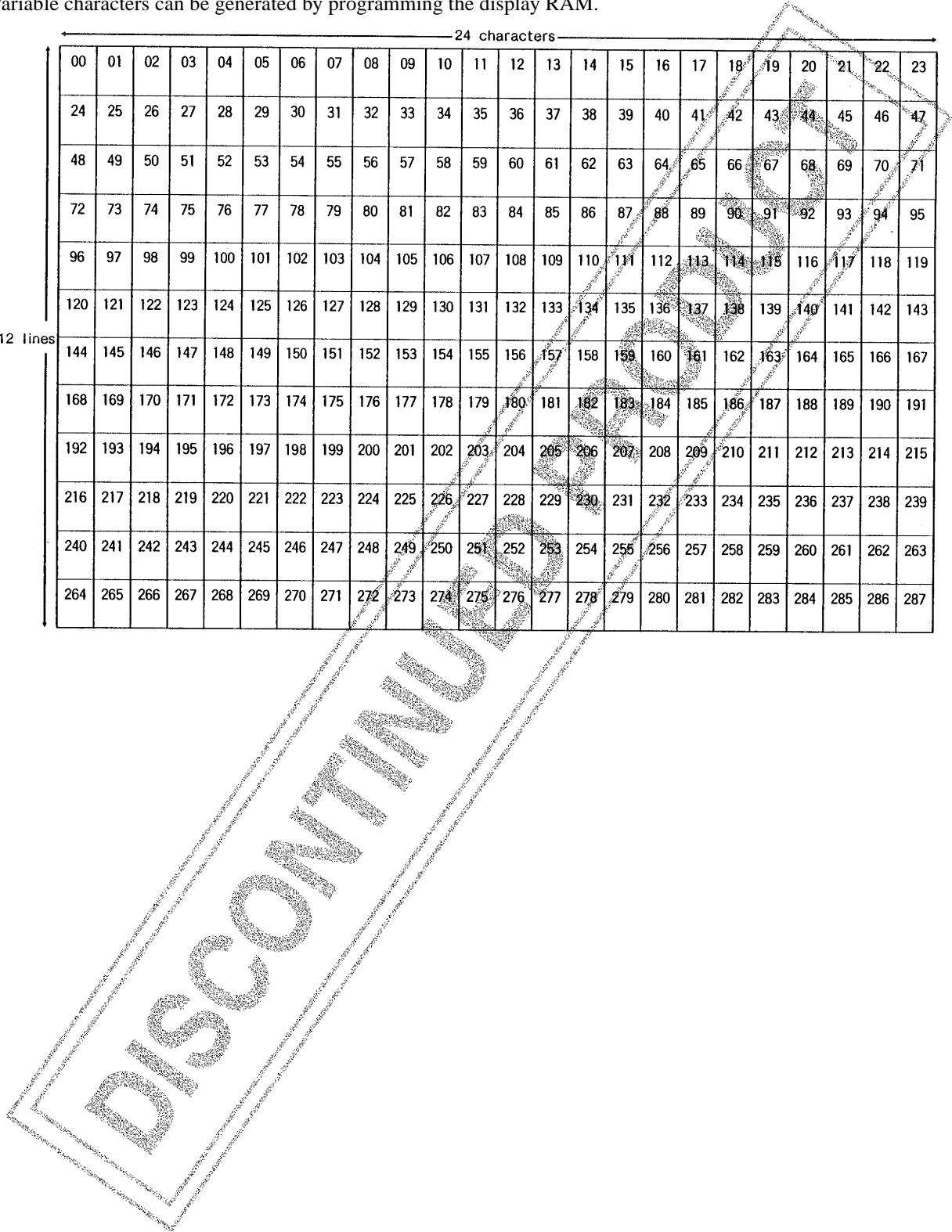


**Display Screen**

The maximum display screen consists of horizontal 24 characters and vertical 12 lines. The number of display characters is 288 (max.). The display characters can consist of display line ROM (12 lines) data and display RAM (176 characters).

- Fixed characters can be specified by making an access to the display line ROM.
- Variable characters can be generated by programming the display RAM.

	← 24 characters →																							
	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23
	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71
	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95
	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119
12 lines	120	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143
	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160	161	162	163	164	165	166	167
	168	169	170	171	172	173	174	175	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191
	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	208	209	210	211	212	213	214	215
	216	217	218	219	220	221	222	223	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239
	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255	256	257	258	259	260	261	262	263
	264	265	266	267	268	269	270	271	272	273	274	275	276	277	278	279	280	281	282	283	284	285	286	287



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## Memory Configuration (display RAM and control RAM)

Memory address and data signals consist of 16 bits.

Address range from 0D (000h) to 175D (0AFh) used as the display RAM.

Address range from 176D (0B0h) to 191D (0BFh) is used as the display control register data area.

Bit Address	DA F	DA E	DA D	DA C	DA B	DA A	DA 9	DA 8	DA 7	DA 6	DA 5	DA 4	DA 3	DA 2	DA 1	DA 0	Remarks
000 (000h)	0	0	0	0	0	0	0	0	BLINK	0	C5	C4	C3	C2	C1	C0	<div style="border: 1px solid black; padding: 5px; display: inline-block;">                     Display RAM area                      Blinking      Character code                 </div>
175 (0AFh)	0	0	0	0	0	0	0	0	BLINK	0	C5	C4	C3	C2	C1	C0	
176 (0B0h)	0	0	0	0	-	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the first line
177 (0B1h)	0	0	0	0	-	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the second line
178 (0B2h)	0	0	0	0	-	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the third line
179 (0B3h)	0	0	0	0	-	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the fourth line
180 (0B4h)	0	0	0	0	-	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the fifth line
181 (0B5h)	0	0	0	0	-	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the sixth line
182 (0B6h)	0	0	0	0	-	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the seventh line
183 (0B7h)	0	0	0	0	-	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the eighth line
184 (0B8h)	0	0	0	0	-	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the ninth line
185 (0B9h)	0	0	0	0	-	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the tenth line
186 (0BAh)	0	0	0	0	-	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the eleventh line
187 (0BBh)	0	0	0	0	-	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the twelfth line
188 (0BCh)	0	0	0	0	HSZ 31	HSZ 30	HSZ 21	HSZ 20	HSZ 11	HSZ 10	HP5	HP4	HP3	HP2	HP1	HP0	Horizontal display position. Horizontal character size.
189 (0BDh)	0	0	0	0	VSZ 31	VSZ 30	VSZ 21	VSZ 20	VSZ 11	VSZ 10	VP5	VP4	VP3	VP2	VP1	VP0	Vertical display position. Vertical character size.
190 (0BEh)	0	0	0	0	INH/ NON	-	-	OSC STP	DSP ON	-	SYS RST	-	-	-	PHASE 1	PHASE 0	Video signal and etc.
191 (0BFh)	0	0	0	0	TSY MOD	-	-	BLK 1	BLK 0	-	BLINK 2	BLINK 1	BLINK 0	EX	-	BCOL	Control register

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## Memory Configuration (display RAM and control RAM)

Memory address and data signals consist of 16 bits.

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Address range from 176D (0B0h) to 191D (0BFh) is used as the display control register data area.

Bit Address	DA F	DA E	DA D	DA C	DA B	DA A	DA 9	DA 8	DA 7	DA 6	DA 5	DA 4	DA 3	DA 2	DA 1	DA 0	Remarks
000 (000h)	0	0	0	0	0	0	0	0	BLINK	0	C5	C4	C3	C2	C1	C0	<div style="border: 1px solid black; padding: 5px; display: inline-block;">                     Blinking                 </div> <div style="border: 1px solid black; padding: 5px; display: inline-block; margin-left: 20px;">                     Character code                 </div> Display RAM area
175 (0AFh)	0	0	0	0	0	0	0	0	BLINK	0	C5	C4	C3	C2	C1	C0	
176 (0B0h)	0	0	0	0	-	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the first line
177 (0B1h)	0	0	0	0	-	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the second line
178 (0B2h)	0	0	0	0	-	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the third line
179 (0B3h)	0	0	0	0	-	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the fourth line
180 (0B4h)	0	0	0	0	-	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the fifth line
181 (0B5h)	0	0	0	0	-	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the sixth line
182 (0B6h)	0	0	0	0	-	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the seventh line
183 (0B7h)	0	0	0	0	-	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the eighth line
184 (0B8h)	0	0	0	0	-	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the ninth line
185 (0B9h)	0	0	0	0	-	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the tenth line
186 (0BAh)	0	0	0	0	-	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the eleventh line
187 (0BBh)	0	0	0	0	-	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the twelfth line
188 (0BCh)	0	0	0	0	HSZ 31	HSZ 30	HSZ 21	HSZ 20	HSZ 11	HSZ 10	HP5	HP4	HP3	HP2	HP1	HP0	Horizontal display position. Horizontal character size.
189 (0BDh)	0	0	0	0	VSZ 31	VSZ 30	VSZ 21	VSZ 20	VSZ 11	VSZ 10	VP5	VP4	VP3	VP2	VP1	VP0	Vertical display position. Vertical character size.
190 (0BEh)	0	0	0	0	INI NON	-	-	OSC STP	DSP ON	-	SYS RST	-	-	-	PHASE 1	PHASE 0	Video signal and etc.
191 (0BFh)	0	0	0	0	TST MOD	-	-	BLK 1	BLK 0	-	BLINK 2	BLINK 1	BLINK 0	EX	-	BCOL	Control register

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## (2) Address 189D (0BD<sub>H</sub>)

DA 0 to C	Register name	Contents		Remarks												
		Status	Function													
0	VP0 (LSB)	0	If a vertical display start position is defined as the VS, the VS can be calculated as follows:  $VS = H \times (4 \sum_{n=0}^5 2^n VP_n)$	<p>The vertical display start position is specified by using six bits VP5 to VP0. The LSB (VP0) has a bit weight of 4H.</p>												
		1			H: Horizontal synchronization pulse cycle											
1	VP1	0														
		1														
2	VP2	0														
		1														
3	VP3	0														
		1														
4	VP4	0														
		1														
5	VP5 (MSB)	0														
		1														
6	VSZ10	0	<table border="1" style="display: inline-table;"> <tr> <td style="border: none;"></td> <td style="border: none;">VSZ10</td> <td style="border: none;">0</td> <td style="border: none;">1</td> </tr> <tr> <td style="border: none;">VSZ11</td> <td style="border: none;">0</td> <td style="border: none;">1T<sub>C</sub>/1 dot</td> <td style="border: none;">2T<sub>C</sub>/1 dot</td> </tr> <tr> <td style="border: none;">1</td> <td style="border: none;">1</td> <td style="border: none;">3T<sub>C</sub>/1 dot</td> <td style="border: none;">4T<sub>C</sub>/1 dot</td> </tr> </table>		VSZ10	0	1	VSZ11	0	1T <sub>C</sub> /1 dot	2T <sub>C</sub> /1 dot	1	1	3T <sub>C</sub> /1 dot	4T <sub>C</sub> /1 dot	Vertical character size for the first line
				VSZ10	0	1										
VSZ11	0	1T <sub>C</sub> /1 dot	2T <sub>C</sub> /1 dot													
1	1	3T <sub>C</sub> /1 dot	4T <sub>C</sub> /1 dot													
1																
7	VSZ11	0														
		1														
8	VSZ20	0	<table border="1" style="display: inline-table;"> <tr> <td style="border: none;"></td> <td style="border: none;">VSZ20</td> <td style="border: none;">0</td> <td style="border: none;">1</td> </tr> <tr> <td style="border: none;">VSZ21</td> <td style="border: none;">0</td> <td style="border: none;">1T<sub>C</sub>/1 dot</td> <td style="border: none;">2T<sub>C</sub>/1 dot</td> </tr> <tr> <td style="border: none;">1</td> <td style="border: none;">1</td> <td style="border: none;">3T<sub>C</sub>/1 dot</td> <td style="border: none;">4T<sub>C</sub>/1 dot</td> </tr> </table>		VSZ20	0	1	VSZ21	0	1T <sub>C</sub> /1 dot	2T <sub>C</sub> /1 dot	1	1	3T <sub>C</sub> /1 dot	4T <sub>C</sub> /1 dot	Vertical character size for the second line
				VSZ20	0	1										
VSZ21	0	1T <sub>C</sub> /1 dot	2T <sub>C</sub> /1 dot													
1	1	3T <sub>C</sub> /1 dot	4T <sub>C</sub> /1 dot													
1																
9	VSZ21	0														
		1														
A	VSZ30	0	<table border="1" style="display: inline-table;"> <tr> <td style="border: none;"></td> <td style="border: none;">VSZ30</td> <td style="border: none;">0</td> <td style="border: none;">1</td> </tr> <tr> <td style="border: none;">VSZ31</td> <td style="border: none;">0</td> <td style="border: none;">1T<sub>C</sub>/1 dot</td> <td style="border: none;">2T<sub>C</sub>/1 dot</td> </tr> <tr> <td style="border: none;">1</td> <td style="border: none;">1</td> <td style="border: none;">3T<sub>C</sub>/1 dot</td> <td style="border: none;">4T<sub>C</sub>/1 dot</td> </tr> </table>		VSZ30	0	1	VSZ31	0	1T <sub>C</sub> /1 dot	2T <sub>C</sub> /1 dot	1	1	3T <sub>C</sub> /1 dot	4T <sub>C</sub> /1 dot	Vertical character size for lines third to twelfth
				VSZ30	0	1										
VSZ31	0	1T <sub>C</sub> /1 dot	2T <sub>C</sub> /1 dot													
1	1	3T <sub>C</sub> /1 dot	4T <sub>C</sub> /1 dot													
1																
B	VSZ31	0														
		1														
C	-	0														
		1														

\*: If the RST pin becomes active (the IC is reset), the contents of all the registers will be set to "0".



# LC7470

## (3) Address 190D (0BE<sub>H</sub>)

DA 0 to C	Register name	Contents				Remarks
		Status	Function			
0	PHASE0	0	PHASE1	PHASE0	Background color	Background color
		1	0	0	$\pi/2$	
1	PHASE1	0	0	1	$\pi$	
		1	1	0	$3\pi/2$	
2	-	0	1	1	In-phase	
		1				
3	-	0				
		1				
4	-	0				
		1				
5	SYSRST	0				With CS pin level=L, the IC is reset. If the pin level changes to H the IC reset will be released
		1	All the registers are reset and the display mode is inactivated			
6	-	0				
		1				
7	DSPON	0	Character OFF			
		1	Character ON			
8	OSCSTP	0	The oscillation circuit does not enter a stop state if the display mode is inactivated			To stop the crystal oscillation circuit and LC oscillation circuit
		1	The oscillation circuit enters the stop state if the display mode is inactivated			
9	-	0				
		1				
A	-	0				
		1				
B	INT/ NON	0	Interlace (262.5H/1 field)			Display operation mode selection: interlace and non-interlace
		1	Non-interlace (263H/1 field)			
C	-	0				
		1				

\*: If the RST pin becomes active (the IC is reset), the contents of all the registers will be set to "0".

## (4) Address 191D (0BF<sub>H</sub>)

DA 0 to C	Register name	Contents				Remarks
		Status	Function			
0	BCOL	0	Active background coloring (available only in internal synchronization mode)			
		1	Inactive background coloring (background level adjustable only)			
1	-	0				
		1				
2	EX	0	External synchronization			HSYNC and VSYNC signals selection: internal and external
		1	Internal synchronization			
3	BLINK0	0	BLINK1 \ BLINK0	0	1	Duty ratio control for blinking mode
		1	0	Blinking OFF mode	Duty: 25%	
4	BLINK1	0	1	Duty: 50%	Duty: 75%	
		1				
5	BLINK2	0	Blinking cycle: 1 second			Blinking cycle control
		1	Blinking cycle: 0.5 second			
6	-	0				
		1				
7	BLK0	0	BLK1 \ BLK0	0	1	Blanking size control
		1	0	Blanking OFF mode	Character size	
8	BLK1	0	1	Partial screen size	Entire screen size	
		1				
9	-	0				
		1				
A	-	0				
		1				
B	TSTMOD	0	Normal operation			Should be fixed to "0"
		1	Test mode			
C	-	0				
		1				

\*: If the RST pin becomes active (the IC is reset), the contents of all the registers will be set to "0".

# LC7470

## Memory Configuration (display line ROM)

The display line ROM address range is from 0D (000<sub>H</sub>) to 1535D (5FF<sub>H</sub>). Data consists of 7 bits.

Bit Address	DA F	DA E	DA D	DA C	DA B	DA A	DA 9	DA 8	DA 7	DA 6	DA 5	DA 4	DA 3	DA 2	DA 1	DA 0	Remarks
000 (000h)	0	0	0	0	0	0	0	0	ROM/RAM	0	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Line ROM: First character of the first line
0023 (017h)	0	0	0	0	0	0	0	0	ROM/RAM	0	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Line ROM: Twenty-fourth character of the first line
0024 (018h)	0	0	0	0	0	0	0	0	ROM/RAM	0	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Line ROM: First character of the second line
1535 (5FFh)	0	0	0	0	0	0	0	0	ROM/RAM	0	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Line ROM: Twenty-fourth character of the sixty-fourth line

DA 0 to 8	Register name	Contents		Remarks							
		Status	Function								
0	ADR0	0	Used to specify the desired character ROM address.  To specify the desired display and control RAM address, set bit 7 (DA7) to '1' and seven bits ADR0 to ADR6 to '0'.  To access the character ROM, addresses 0D (000) to 63D (3F <sub>H</sub> ) can be used.  Set bit 6 (ADR6) to '0'.  Direct read access to the character ROM. Read access to the character ROM through the display RAM								
		1									
1	ADR1	0		Used to specify the desired character ROM address.  To specify the desired display and control RAM address, set bit 7 (DA7) to '1' and seven bits ADR0 to ADR6 to '0'.  To access the character ROM, addresses 0D (000) to 63D (3F <sub>H</sub> ) can be used.  Set bit 6 (ADR6) to '0'.  Direct read access to the character ROM. Read access to the character ROM through the display RAM							
		1									
2	ADR2	0			Used to specify the desired character ROM address.  To specify the desired display and control RAM address, set bit 7 (DA7) to '1' and seven bits ADR0 to ADR6 to '0'.  To access the character ROM, addresses 0D (000) to 63D (3F <sub>H</sub> ) can be used.  Set bit 6 (ADR6) to '0'.  Direct read access to the character ROM. Read access to the character ROM through the display RAM						
		1									
3	ADR3	0				Used to specify the desired character ROM address.  To specify the desired display and control RAM address, set bit 7 (DA7) to '1' and seven bits ADR0 to ADR6 to '0'.  To access the character ROM, addresses 0D (000) to 63D (3F <sub>H</sub> ) can be used.  Set bit 6 (ADR6) to '0'.  Direct read access to the character ROM. Read access to the character ROM through the display RAM					
		1									
4	ADR4	0					Used to specify the desired character ROM address.  To specify the desired display and control RAM address, set bit 7 (DA7) to '1' and seven bits ADR0 to ADR6 to '0'.  To access the character ROM, addresses 0D (000) to 63D (3F <sub>H</sub> ) can be used.  Set bit 6 (ADR6) to '0'.  Direct read access to the character ROM. Read access to the character ROM through the display RAM				
		1									
5	ADR5	0						Used to specify the desired character ROM address.  To specify the desired display and control RAM address, set bit 7 (DA7) to '1' and seven bits ADR0 to ADR6 to '0'.  To access the character ROM, addresses 0D (000) to 63D (3F <sub>H</sub> ) can be used.  Set bit 6 (ADR6) to '0'.  Direct read access to the character ROM. Read access to the character ROM through the display RAM			
		1									
6	ADR6	0							Used to specify the desired character ROM address.  To specify the desired display and control RAM address, set bit 7 (DA7) to '1' and seven bits ADR0 to ADR6 to '0'.  To access the character ROM, addresses 0D (000) to 63D (3F <sub>H</sub> ) can be used.  Set bit 6 (ADR6) to '0'.  Direct read access to the character ROM. Read access to the character ROM through the display RAM		
		1									
7	ROM/RAM	0								Used to specify the desired character ROM address.  To specify the desired display and control RAM address, set bit 7 (DA7) to '1' and seven bits ADR0 to ADR6 to '0'.  To access the character ROM, addresses 0D (000) to 63D (3F <sub>H</sub> ) can be used.  Set bit 6 (ADR6) to '0'.  Direct read access to the character ROM. Read access to the character ROM through the display RAM	
		1									

## Display Line ROM: Line Address Table

Line No.	Address No.	Line No.	Address No.
1st line	00 <sub>HEX</sub> (0000)	33rd line	300 <sub>HEX</sub> (0768)
2nd line	18 <sub>HEX</sub> (0024)	34th line	318 <sub>HEX</sub> (0792)
3rd line	30 <sub>HEX</sub> (0048)	35th line	330 <sub>HEX</sub> (0816)
4th line	48 <sub>HEX</sub> (0072)	36th line	348 <sub>HEX</sub> (0840)
5th line	60 <sub>HEX</sub> (0096)	37th line	360 <sub>HEX</sub> (0864)
6th line	78 <sub>HEX</sub> (0120)	38th line	378 <sub>HEX</sub> (0888)
7th line	90 <sub>HEX</sub> (0144)	39th line	390 <sub>HEX</sub> (0912)
8th line	A8 <sub>HEX</sub> (0168)	40th line	3A8 <sub>HEX</sub> (0936)
9th line	C0 <sub>HEX</sub> (0192)	41st line	3C0 <sub>HEX</sub> (0960)
10th line	D8 <sub>HEX</sub> (0216)	42nd line	3D8 <sub>HEX</sub> (0984)
11th line	F0 <sub>HEX</sub> (0240)	43rd line	3F0 <sub>HEX</sub> (1008)
12th line	108 <sub>HEX</sub> (0264)	44th line	408 <sub>HEX</sub> (1032)
13th line	120 <sub>HEX</sub> (0288)	45th line	420 <sub>HEX</sub> (1056)
14th line	138 <sub>HEX</sub> (0312)	46th line	438 <sub>HEX</sub> (1080)
15th line	150 <sub>HEX</sub> (0336)	47th line	450 <sub>HEX</sub> (1104)
16th line	168 <sub>HEX</sub> (0360)	48th line	468 <sub>HEX</sub> (1128)
17th line	180 <sub>HEX</sub> (0384)	49th line	480 <sub>HEX</sub> (1152)
18th line	198 <sub>HEX</sub> (0408)	50th line	498 <sub>HEX</sub> (1176)
19th line	1B0 <sub>HEX</sub> (0432)	51st line	4B0 <sub>HEX</sub> (1200)
20th line	1C8 <sub>HEX</sub> (0456)	52nd line	4C8 <sub>HEX</sub> (1224)
21st line	1E0 <sub>HEX</sub> (0480)	53rd line	4E0 <sub>HEX</sub> (1248)
22nd line	1F8 <sub>HEX</sub> (0504)	54th line	4F8 <sub>HEX</sub> (1272)
23rd line	210 <sub>HEX</sub> (0528)	55th line	510 <sub>HEX</sub> (1296)
24th line	228 <sub>HEX</sub> (0552)	56th line	528 <sub>HEX</sub> (1320)
25th line	240 <sub>HEX</sub> (0576)	57th line	540 <sub>HEX</sub> (1344)
26th line	258 <sub>HEX</sub> (0600)	58th line	558 <sub>HEX</sub> (1368)
27th line	270 <sub>HEX</sub> (0624)	59th line	570 <sub>HEX</sub> (1392)
28th line	288 <sub>HEX</sub> (0648)	60th line	588 <sub>HEX</sub> (1416)
29th line	2A0 <sub>HEX</sub> (0672)	61st line	5A0 <sub>HEX</sub> (1440)
30th line	2B8 <sub>HEX</sub> (0696)	62nd line	5B8 <sub>HEX</sub> (1464)
31st line	2D0 <sub>HEX</sub> (0720)	63rd line	5D0 <sub>HEX</sub> (1488)
32nd line	2E8 <sub>HEX</sub> (0744)	64th line	5E8 <sub>HEX</sub> (1512)

Sample Display Screen

Twelve display lines of the display 64-line ROM are specified. Variable characters are prepared in the display control RAM. The display RAM address area is automatically allocated to addresses from 0D (000H) to 175D (AFH) in the display order.

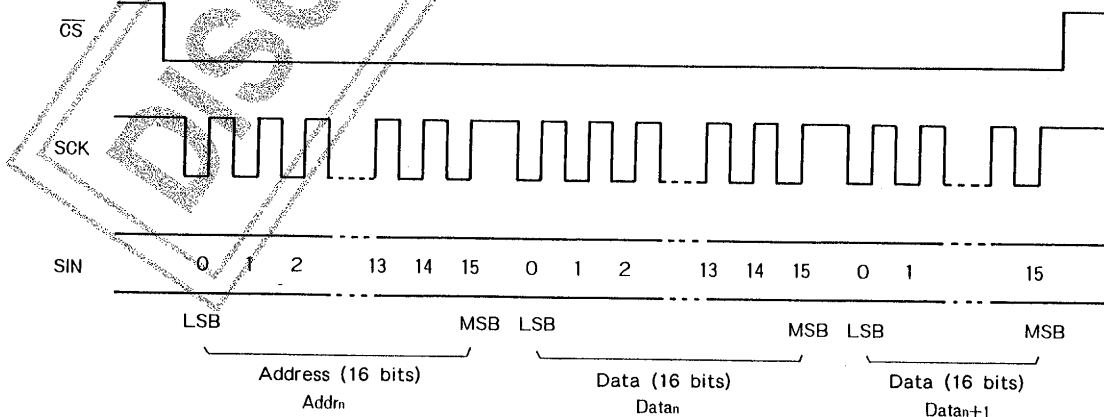
- The display characters indicated by bold lines are specified through the display RAM access.
- The display characters indicated by slender lines are specified directly through the display ROM access.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
1	ROM 000h	ROM 001h	ROM 002h	ROM 003h	ROM 004h	ROM 005h	ROM 006h	ROM 007h	ROM 008h	ROM 009h	ROM 010h	ROM 011h	ROM 012h	ROM 013h	ROM 014h	RAM 000h	RAM 001h	RAM 002h	RAM 003h	RAM 004h	RAM 005h	ROM 007h	ROM 008h	ROM 009h
2	ROM 024h	RAM 006h	RAM 007h	RAM 008h	RAM 009h	ROM 010h	ROM 030h	ROM 031h	ROM 032h	ROM 033h	RAM 010h	RAM 011h	RAM 012h	RAM 013h	RAM 014h	RAM 015h	RAM 016h	RAM 017h	RAM 018h	RAM 019h	RAM 020h	RAM 021h	RAM 022h	RAM 023h
3	RAM 048h	RAM 049h	RAM 050h	RAM 051h	RAM 052h	RAM 053h	RAM 054h	RAM 055h	RAM 056h	RAM 057h	RAM 058h	RAM 059h	RAM 060h	RAM 061h	RAM 062h	RAM 063h	RAM 064h	RAM 065h	RAM 066h	RAM 067h	RAM 068h	RAM 069h	RAM 070h	RAM 071h
4	ROM 072h	ROM 073h	ROM 074h	ROM 075h	ROM 076h	RAM 077h	RAM 078h	RAM 079h	RAM 080h	RAM 081h	RAM 082h	RAM 083h	RAM 084h	RAM 085h	RAM 086h	RAM 087h	RAM 088h	RAM 089h	RAM 090h	RAM 091h	RAM 092h	RAM 093h	RAM 094h	RAM 095h
5	ROM 086h	RAM 041h	RAM 042h	RAM 043h	RAM 044h	RAM 045h	RAM 046h	RAM 047h	RAM 048h	ROM 105h	RAM 049h	RAM 050h	RAM 051h	RAM 052h	RAM 053h	RAM 054h	RAM 055h	RAM 056h	RAM 057h	RAM 058h	RAM 059h	RAM 060h	RAM 061h	RAM 062h
6	ROM 120h	RAM 065h	RAM 066h	RAM 067h	RAM 068h	RAM 069h	RAM 070h	RAM 071h	RAM 072h	RAM 073h	RAM 074h	RAM 075h	RAM 076h	RAM 077h	RAM 078h	RAM 079h	RAM 080h	RAM 081h	RAM 082h	RAM 083h	RAM 084h	RAM 085h	RAM 086h	RAM 087h
7	RAM 073h	RAM 074h	RAM 075h	RAM 076h	RAM 077h	RAM 078h	RAM 079h	RAM 080h	RAM 081h	RAM 082h	RAM 083h	RAM 084h	RAM 085h	RAM 086h	RAM 087h	RAM 088h	RAM 089h	RAM 090h	RAM 091h	RAM 092h	RAM 093h	RAM 094h	RAM 095h	RAM 096h
8	RAM 085h	RAM 086h	RAM 087h	RAM 088h	RAM 089h	RAM 090h	RAM 091h	RAM 092h	RAM 093h	RAM 094h	RAM 095h	RAM 096h	RAM 180h	RAM 181h	RAM 182h	RAM 183h	RAM 184h	RAM 185h	RAM 186h	RAM 187h	RAM 188h	RAM 189h	RAM 190h	RAM 191h
9	ROM 192h	ROM 193h	ROM 194h	ROM 195h	ROM 196h	ROM 197h	ROM 198h	ROM 199h	ROM 200h	ROM 201h	ROM 202h	ROM 203h	RAM 087h	RAM 088h	RAM 089h	RAM 090h	RAM 091h	RAM 092h	RAM 093h	RAM 094h	RAM 095h	RAM 096h	RAM 097h	RAM 098h
10	ROM 216h	ROM 217h	ROM 218h	ROM 219h	ROM 220h	RAM 108h	RAM 110h	RAM 111h	RAM 112h	RAM 113h	RAM 114h	RAM 115h	RAM 116h	RAM 117h	RAM 118h	RAM 119h	RAM 120h	RAM 121h	RAM 122h	RAM 123h	RAM 124h	RAM 125h	RAM 126h	RAM 127h
11	ROM 240h	ROM 241h	ROM 242h	ROM 243h	ROM 244h	RAM 135h	RAM 137h	RAM 138h	RAM 139h	RAM 140h	RAM 141h	RAM 142h	RAM 143h	RAM 144h	RAM 145h	RAM 146h	RAM 147h	RAM 148h	RAM 149h	RAM 150h	RAM 151h	RAM 152h	RAM 153h	RAM 154h
12	RAM 159h	RAM 160h	RAM 161h	RAM 162h	RAM 163h	RAM 164h	RAM 165h	RAM 166h	RAM 167h	RAM 168h	RAM 169h	RAM 170h	RAM 171h	RAM 172h	RAM 173h	RAM 174h	RAM 175h	RAM 176h	RAM 177h	RAM 178h	RAM 179h	RAM 180h	RAM 181h	RAM 182h

Input Timings of External Control Data

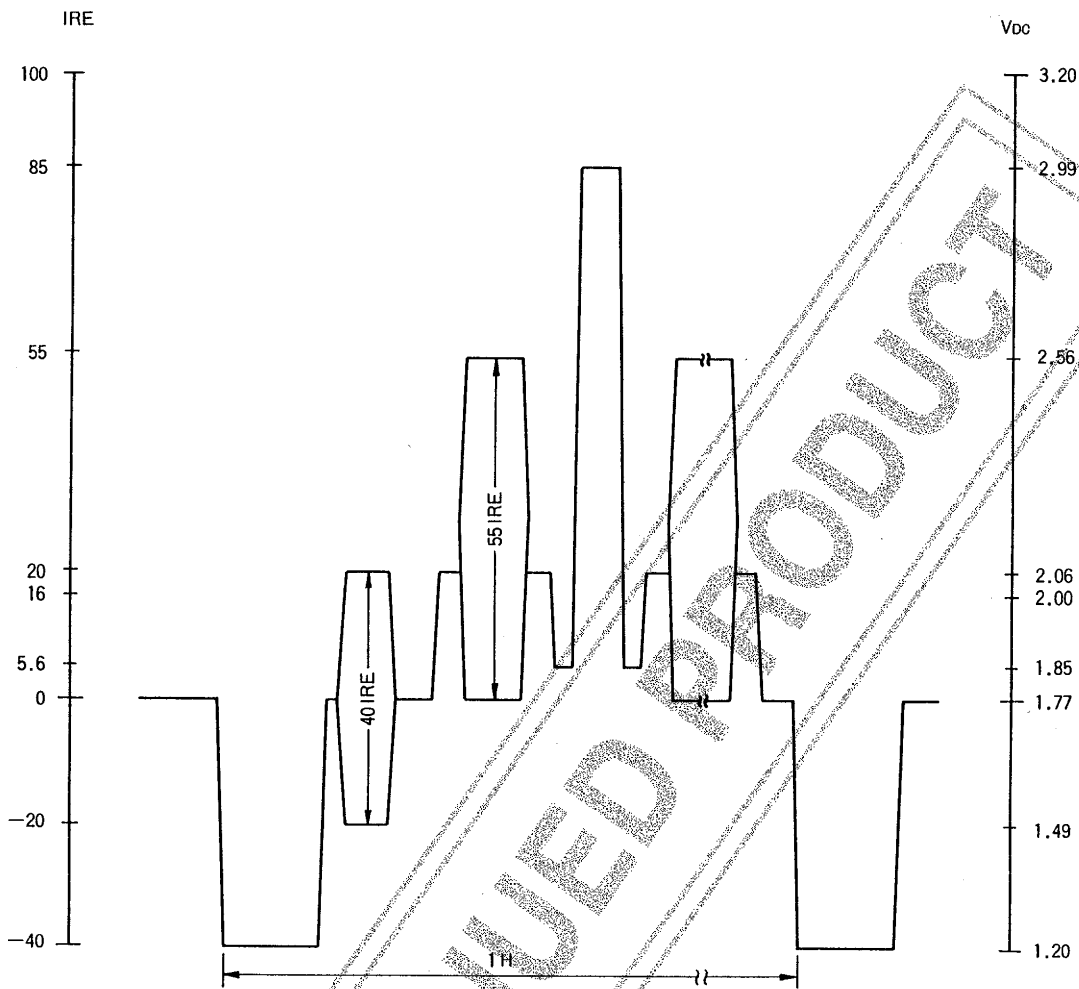
Address and data information is input serially to this chip from an external device.

- (1) Address data consist of 16 bits.  
The 8 low-order bits have significance. Always set 8 high-order bits to '0'.
- (2) Data consists of 16 bits.
  - Only 8 low-order bits of input data to addresses from 000H to 0AFH have significance. Always set 8 high-order bits to '0'.
  - Only 11 low-order bits of input data to addresses from 0B0H to 0BBH have significance. Always set 5 high-order bits to '0'.
  - Only 12 low-order bits of input data to addresses from 0BCH to 0BFH have significance. Always set 4 high-order bits to '0'.
- (3) The data input format is shown below. The first 16 bits after the  $\overline{CS}$  pin (active low) becomes active are processes as an address data. The subsequent groups of 16 bits are handled as the data.



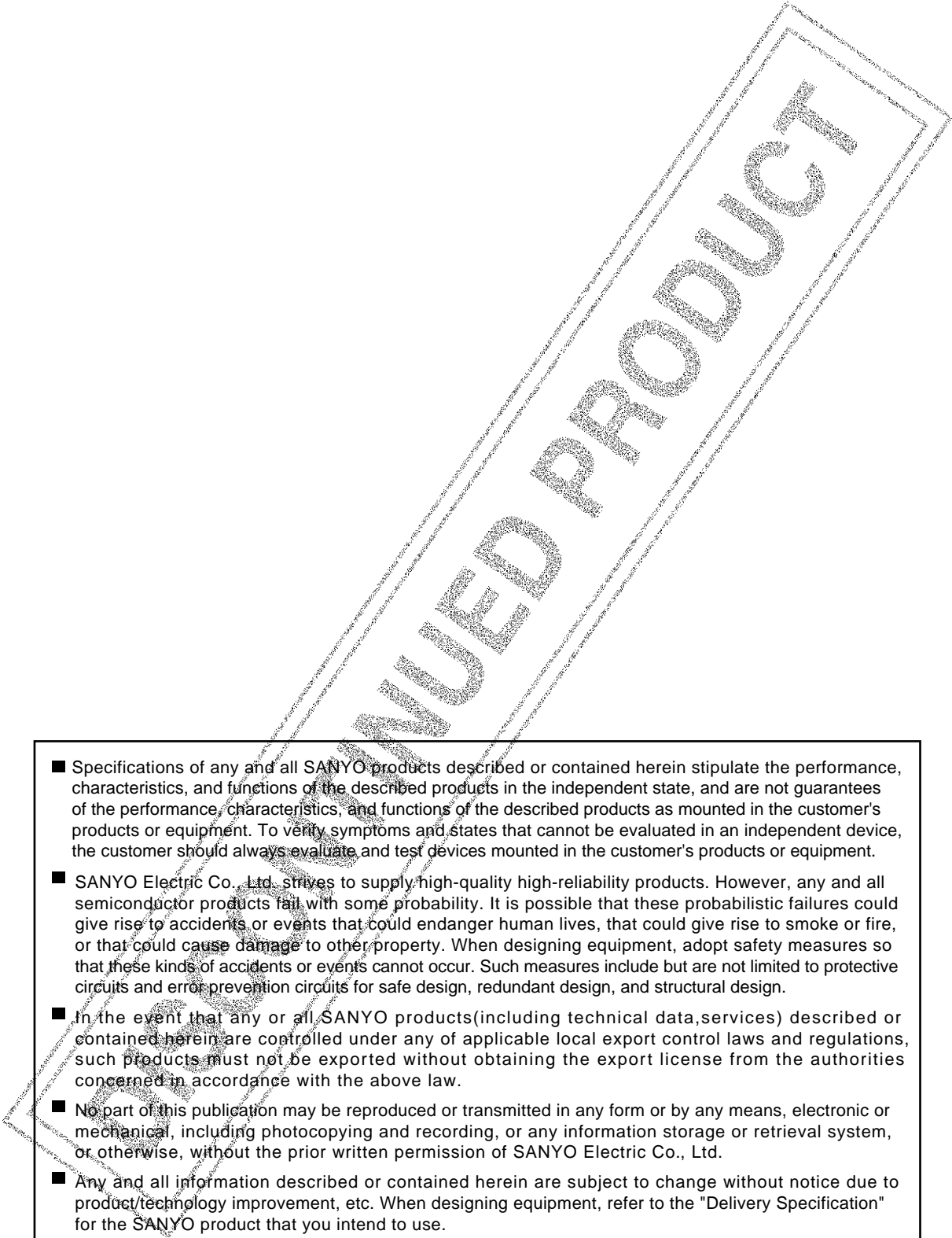
# LC7470

## Composite Video Signal Output Level (Internal Generation)



Output level (IRE)	Output voltage (VDC)
100	3.200
85	2.986
46.1	2.430
20	2.057
5.8	1.854
0	1.771
-20	1.486
-40	1.200

$V_{DD}=5.000V_{DC}$

- 
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