An6866

DOT MATRIX LCD CONTROLLER & DRIVER

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FUNCTION

- Character type dot matrix LCD controller and driver
- Easy Interface with 4-bit or 8-bit microprocessors
- Wide range of various instruction functions
- Standard and extended operation modes for applications flexibility
- Mask programming of extended functions in standard/extended modes according to the Order Form
- Mask programming of the desired customer's characters table
- 1 line of 5x8 or 5x11 dot or 2 lines of 5x8 dot characters display
- Chip and Mode Identifier allows to detect chip version and current state of controller
- Internal driver: 16 common and 40 segment signal outputs
- Interface with the An6865 or An6863 extension driver to increase number of displayed characters (up to 80)
- Build-in automatic power-on reset function
- Internal oscillator with one external resistor
- Chip version configured with on-chip LCD supply voltage bias resistors and a clock oscillator resistor (no additional external elements)

FEATURES

- Power Supply Voltage: 2.7V to 5.5V
- LCD Driving Voltage: 3.0V to 13V
- Two types of Display Waveforms:
  - A-type (line inversion)
  - B-type (frame inversion)
- High-speed MPU bus interface - 2 MHz (at 5V Power Supply)
- Display Data RAM size is 80 x 8 bits for 80 characters
- Character Generator ROM size is 19840 bits with two pages:
  - 2 pages with 240 characters of 5x8 dot format for each or
  - 1 page with 240 5x11 dot characters or
  - combination of 2 pages region with 5x8 dot characters and 1 page region with 5x11 dot characters
- Character Generator RAM size is 64 x 8 bits for:
  - 8 characters of 5x8 dot format or
  - 4 characters of 5x11 dot format
- Programmable duty cycle:
  - 1/8 duty for one line of 5x8 dot characters
  - 1/11 duty for one line of 5x11 dot characters
  - 1/16 duty for two lines of 5x8 dot characters
- Low power consumption

Ordering Information

Version	Description
An6866-xxyy	Controller version with full function set for Standard and Extended modes
An6866S-xxyy	Controller version only for Standard mode (XMODE=1 or NC)

Note: xx – Functional mask option number,
yy – CGROM pattern number

INTRODUCTION

The An6866 is a dot matrix LCD controller designed for display of alphanumeric data. It has standard compatible mode and extended mode with larger CGROM size and additional service functions.

The An6866 has 16 COM and 40 SEG outputs to display one 5x8 or 5x11 dot character line, or two 5x8 dot character lines. With internal segment outputs the controller can display up to 8 characters in each line (up to 16 characters in two-line mode). Extension drivers increase number of displayed characters to 80 (up to 40 characters in a line for two-line mode).

The displayed character codes are written into the 80-byte Display Data RAM (DDRAM). Character patterns are stored in the 19,840-bit Character Generator ROM (CGROM) or 64x8-bit Character Generator RAM (CGRAM). The CGROM capacity allows to code two pages of 5x8 dot characters or one 5x11 dot character page (up to 248 characters on each page). Mixed format coding is also allowed. In the CGRAM the user can write eight 5x8 dot characters or four 5x11 dot characters.

Data exchange with an external control device is performed by an easy-to-use system interface compatible with many MPU types. Also the controller has a wide instruction set. Instructions and data can be transferred via 4- or 8-bit data bus. The An6866 features an advanced 4-bit interface that allows synchronization of the internal controller state with the interface timing diagram.

The An6866 has a standard extension driver interface with An6865, An6863 and similar type drivers. COM and SEG waveforms can be "A" or "B" type, as selected in the Order Form.

Reset function initializes the controller automatically after power on.

The An6866 has a Chip and Mode IDentifier (CMID), that allows the external MPU to detect chip version, ROM code and service functions status, as well as the current operation mode, and to adjust the system operating according to received data.

The controller is fabricated by the production single-metal CMOS technology. Mask programming of the CGROM, as well as initialization state, and the extended functions selection, are implemented by metal mask.

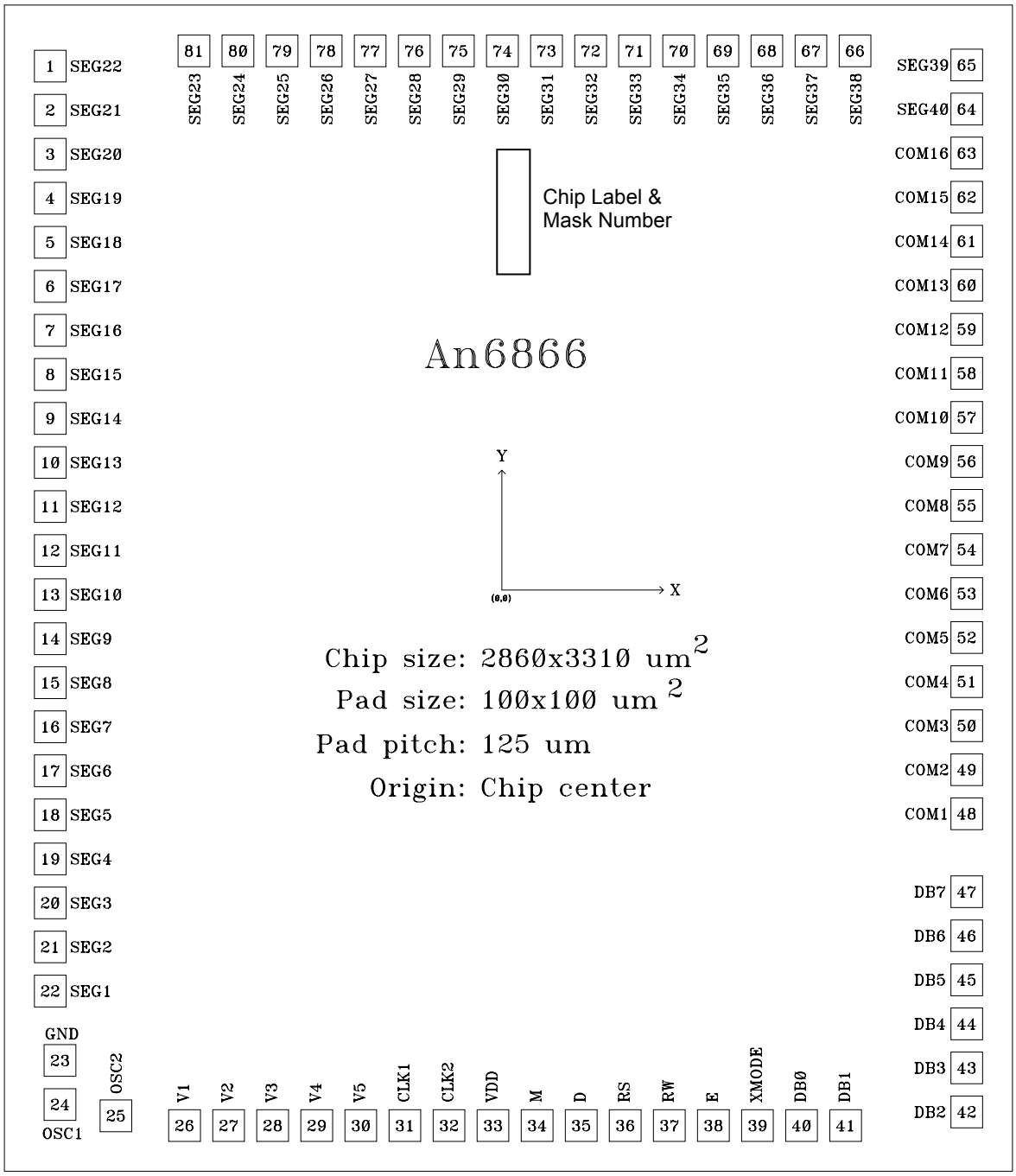
The controller IC contains on-chip LCD supply voltage bias resistors and a clock oscillator resistor. Whether the on-chip resistors should be connected as well as their nominal resistances are selected by the customer when making an order for a mask option.

Therefore, the An6866 features two base operation modes*):

1) **The Standard compatible mode with basic function set. This mode is enabled when the XMODE pin is either not connected or set to the logic "1" state.**
2) **The Extended mode, allows to use extended functions. This mode is enabled when the XMODE pin is connected to GND or set to the logic "0" state. The extended functions include the use of two CGROM pages for 5x8 dot characters, the Display Inversion control capability, the cursor blinking mode (similar to the PC text mode cursor).**

***) Note: Standard and Extended functions as well as CGROM character coding and the initial state after power on can be selected by the Customer when filling in the Order Form. Some functions can be made accessible in the Standard mode, others in the Extended mode. Certain functions can be accessible in both modes or disabled (see Order Form).**

PAD DIAGRAM


1 SEG22
2 SEG21
3 SEG20
4 SEG19
5 SEG18
6 SEG17
7 SEG16
8 SEG15
9 SEG14
10 SEG13
11 SEG12
12 SEG11
13 SEG10
14 SEG9
15 SEG8
16 SEG7
17 SEG6
18 SEG5
19 SEG4
20 SEG3
21 SEG2
22 SEG1
GND 23
24 OSC1
OSC2 25
81 SEG23
80 SEG24
79 SEG25
78 SEG26
77 SEG27
76 SEG28
75 SEG29
74 SEG30
73 SEG31
72 SEG32
71 SEG33
70 SEG34
69 SEG35
68 SEG36
67 SEG37
66 SEG38
SEG39 65
SEG40 64
COM16 63
COM15 62
COM14 61
COM13 60
COM12 59
COM11 58
COM10 57
COM9 56
COM8 55
COM7 54
COM6 53
COM5 52
COM4 51
COM3 50
COM2 49
COM1 48
DB7 47
DB6 46
DB5 45
DB4 44
DB3 43
DB2 42
V1 26
V2 27
V3 28
V4 29
V5 30
CLK1 31
CLK2 32
VDD 33
M 34
D 35
RS 36
RW 37
E 38
XMODE 39
DB0 40
DB1 41
Chip Label &
Mask Number
An6866
Y
X
(0,0)
Chip size: 2860x3310 um2
Pad size: 100x100 um2
Pad pitch: 125 um
Origin: Chip center

PAD LOCATION COORDINATES

Pad No	Pad Name	Coordinates		Pad No	Pad Name	Coordinates	
		X (μm)	Y (μm)			X (μm)	Y (μm)
1	SEG22	135.0	3136.9	42	DB2	2725.0	168.7
2	SEG21		3011.9	43	DB3		293.7
3	SEG20		2886.9	44	DB4		418.7
4	SEG19		2761.9	45	DB5		543.7
5	SEG18		2636.9	46	DB6		668.7
6	SEG17		2511.9	47	DB7		793.7
7	SEG16		2386.9	48	COM1		1015.0
8	SEG15		2261.9	49	COM2		1140.0
9	SEG14		2136.9	50	COM3		1265.0
10	SEG13		2011.9	51	COM4		1390.0
11	SEG12		1886.9	52	COM5		1515.0
12	SEG11		1761.9	53	COM6		1640.0
13	SEG10		1636.9	54	COM7		1765.0
14	SEG9		1511.9	55	COM8		1890.0
15	SEG8		1386.9	56	COM9		2015.0
16	SEG7		1261.9	57	COM10		2140.0
17	SEG6		1136.9	58	COM11		2265.0
18	SEG5		1011.9	59	COM12		2390.0
19	SEG4		886.9	60	COM13		2515.0
20	SEG3		761.9	61	COM14		2640.0
21	SEG2		636.9	62	COM15		2765.0
22	SEG1		511.9	63	COM16		2890.0
23	GND	162.9	314.8	64	SEG40		3015.0
24	OSC1	162.9	189.8	65	SEG39		3140.0
25	OSC2	316.3	162.9	66	SEG38	2412.6	3175.0
26	V1	511.0	135.0	67	SEG37	2287.6	
27	V2	636.0		68	SEG36	2162.6	
28	V3	761.0		69	SEG35	2037.6	
29	V4	886.0		70	SEG34	1912.6	
30	V5	1011.0		71	SEG33	1787.6	
31	CLK1	1136.0		72	SEG32	1662.6	
32	CLK2	1261.0		73	SEG31	1537.6	
33	VDD	1386.0		74	SEG30	1412.6	
34	M	1511.0		75	SEG29	1287.6	
35	D	1636.0		76	SEG28	1162.6	
36	RS	1761.0		77	SEG27	1037.6	
37	RW	1886.0		78	SEG26	912.6	
38	E	2011.0		79	SEG25	787.6	
39	XMODE	2136.0		80	SEG24	662.6	
40	DB0	2261.0		81	SEG23	537.6	
41	DB1	2386.0					

PIN DESCRIPTION

Pin Name	Lines	Input/output	Description	Interface
V_{DD}	1	-	Positive voltage for logical circuit and LCD drivers	Power supply
GND	1	-	Ground (0V)	Power supply
V1 - V5	5	-	Bias voltage level for LCD driving from Power supply or resistive divider: $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$. V_5 – negative bias voltage: V_{DD}-V_5=V_{LCD}.	Power supply
COM1 - COM16	16	output	Common signal outputs for LCD driving	LCD
SEG1 - SEG40	40	output	Segment signal outputs for LCD driving	
OSC1, OSC2	2	input OSC1 output OSC2	When using internal oscillator, connect external resistor. If external clock is used, connect it to OSC1 (OSC2 open).	external resistor or external oscillator
CLK1	1	output	Extension driver latch clock	Extension driver
CLK2	1	output	Extension driver shift clock	
M	1	output	The alternating signal to change polarity of LCD driver voltage.	
D	1	output	Output extension driver data.	
RS	1	input (pull-up to V_{DD})	Used as Interface register selection input. When RS=1 Data register is selected. When RS=0 Instruction register is selected (when writing) or Busy flag state and current address (when reading).	MPU
RW	1	input (pull-up to V_{DD})	Used as read/write selection input. When RW=1 - reading operation When RW=0 – writing operation.	
E	1	input	Used as read/write enable signal.	
DB0 - DB3	4	input / output (pull-up to V_{DD})	Used as low order bi-directional data bus, when 8 bit bus mode. Not used, when 4-bit bus mode.	
DB4 - DB7	4	input / output (pull-up to V_{DD})	Used as high order bi-directional data bus, when 8-bit bus mode. Used as both high and low order, when 4-bit bus mode pins are. DB7 used for Busy flag output.	
XMODE	1	input (pull-up to V_{DD})	Used as operation mode switch signal: XMODE=1 – standard mode, XMODE=0 – extended mode.	MPU or control circuit

FUNCTIONAL DESCRIPTION OF AN6866

1. OVERVIEW

The An6866 internally provides all necessary functions to display characters. The chip includes interface with MPU, DDRAM, CGRAM and CGROM, LCD drivers and extended drivers interface to increase number of displaying characters. This controller allows to build information displaying systems with minimum of external components. It is possible to display one line with 5x8 or 5x11 characters or two lines with 5x8 characters.

Block Diagram is shown in Figure 1.

The An6866 is controlled by instructions from MPU interface. The Interface contains 8-bit data bus DB[7..0], interface operation enable pin (E), read/write mode pin (RW), data register or instructions register select pin (RS).

The controller can interface with MPU by two ways:

- by using 8-bit data bus and 3 control signals (totally 11 interface lines);
- by using 4 high-order bits of data bus (totally 7 interface lines), thus 4-bit data transferred twice (with two E pulses). For increase reliability of data transferring special synchronization mechanism for 4-bit groups is used.

The controller is operated through 2 input buffer registers: IR (Instruction Register) and DR (Data Register). Instructions and data are written into the selected register with E fall, then interface is locked out for the instruction execution time. Instructions are executed according to internal timing diagram independently of interface functioning. Busy Flag (BF) is used to check the state of current instruction execution. Before sending the next instruction to the controller, the MPU must check BF and make sure that previous instruction is finished and input registers are open for new data and instructions.

This interface model allows to operate with high-frequency bus independently from slow internal timing diagram of the controller, which forms internal cycles of instruction executing, memory access and display waveform.

Each instruction execution is accompanied with data reading from internal memory into output Data Register (DR). MPU can read this data by the next Data Read instruction.

The controller has 4 classes of instructions:

- designate controller functions (Function Set, Entry Mode Set, Display Clear, Display on/off, Cursor on/off, Blinking on/off);
- set internal RAM addresses (Set DDRAM/CGRAM Address, Return Home);
- perform data reading/writing operations with internal memory;
- perform miscellaneous functions.

Controller contains 3 memory units:

- DDRAM: contains codes of displayed characters (80 bytes). Character order in DDRAM corresponds to character order on LCD;
- CGROM: contains font table. CGROM contains up to 240 (248) characters at code range 16 (8) to 255. Coding of 5x8 or 5x11 dot characters is available, 5x8 dot characters may be allocated in two pages.
- CGRAM with 64-byte capacity for user characters (totally 8 characters 5x8 dots or 4 characters 5x11 dots). CGRAM occupies 16 (8) character codes from 0 to 15 (7). If CGRAM or its part is not used for user characters, it may be used as general purpose RAM.

Chip and Mode Identifier (CMID) allows external device to read type, chip version and current state of the controller. CMID allows to increase system functionality and reliability.

Controller memory (DDRAM or CGRAM) is allocated according to the current address stored in Address Counter (AC). It means that before random access to memory, it is necessary to write Set CGRAM/DDRAM Address instruction. After execution of any read/write instruction, AC address automatically changes by 1. Direction of AC address change depends on "ID" control bit of Entry Mode Set instruction.

Address Counter also defines cursor position on LCD.

The controller also has mode in which data write combines with display shift. It means that character code writing into DDRAM, address autoincrement and display backward shift take place simultaneously. Visually the cursor is stable and the character line is shifting. This mode is enabled by "S" control bit of "Entry mode Set" instruction.

Autoincrement feature allows to simplify controller programming for end-user applications.

DDRAM addressing depends on display format. In 1-line mode, single address range from 0 to 79 for all 80 characters is used. In 2-line mode, DDRAM address is divided into two ranges: from 0 to 39 for the first line and from 64 to 103 for the second line. When sequential incrementing or decrementing of AC address counter, DDRAM address passes both ranges, accordingly the cursor moves from the first line to the second and vice versa.

Character code read from DDRAM during display refresh time is used to select its pattern from the CGROM or CGRAM. Data from Character Generator is transformed to sequential form and written into SEG shift register at each CLK2 strobe. When SEG shift register if filled with data for the next COM (display row), data is transferred from shift register to SEG outputs latches at CLK1 strobe synchronously with switching to the next COM, and data appears in all driver outputs and on the LCD.

The controller has 40 SEG (display column) drivers for displaying first 8 characters per line. To increase number of displayed characters, it is possible to use extension drivers such as An6865 (40 SEG) or An6863 (80 SEG). Extension drivers are connected to the controller through driver interface, which contains 4 outputs:

- CLK2 – data shift strobe,
- CLK1 – data latch strobe,
- D – serial data output for shift register extension,
- M – alternating signal for polarity change of LCD voltage.

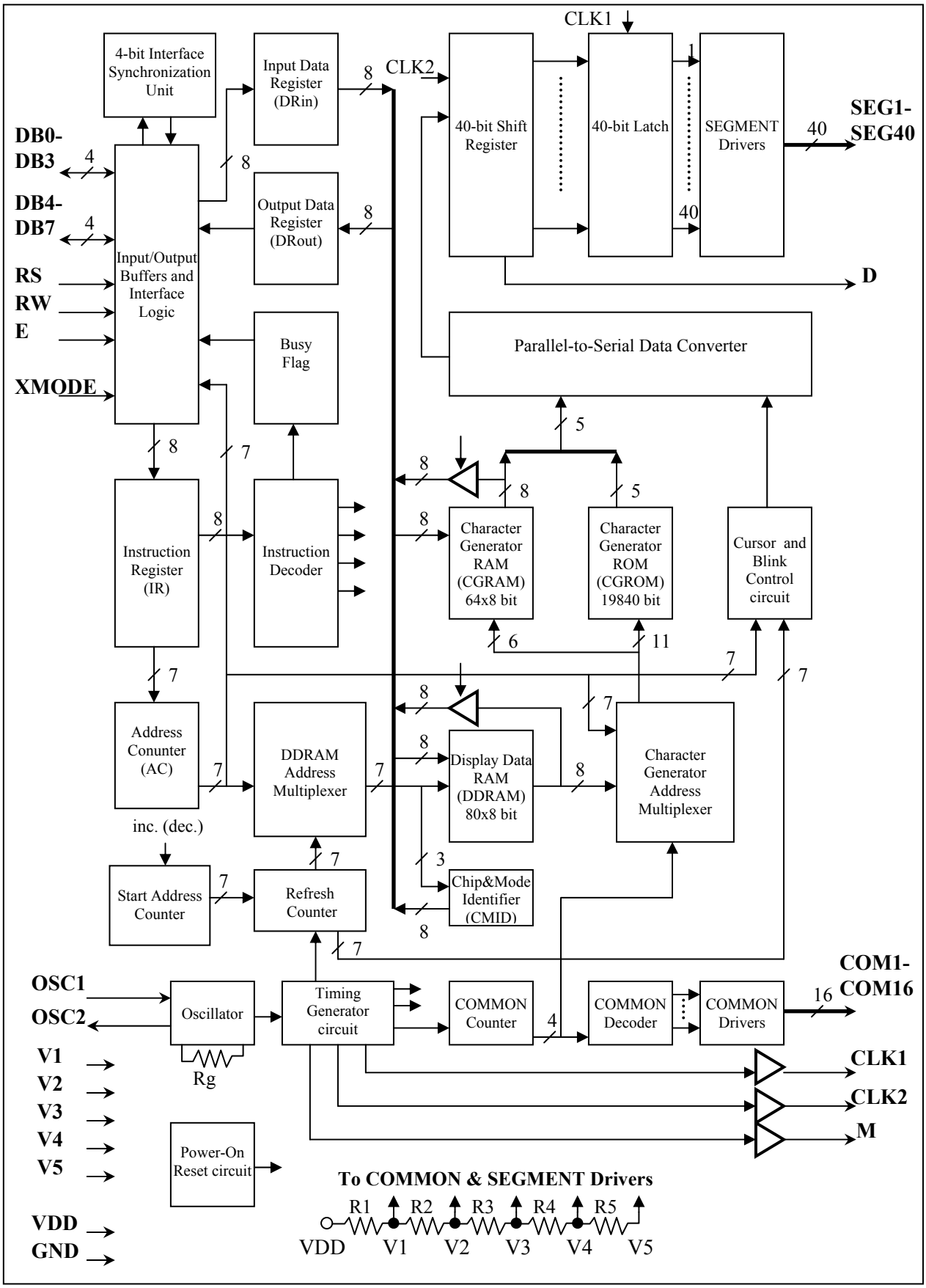


Figure 1. An6866 Block Diagram.

Functional diagram can be divided into the following parts:

1) **Logic control circuit:**
   - MPU bus interface,
   - Instruction decoder,
   - Address Counter (AC),
   - Start Address Counter,
   - Oscillator and Timing generator,
   - Timers for COM cycle and character/cursor blinking,
   - Cursor forming circuit,
   - Power-on Reset circuit.
2) **Memory circuit:**
   - Display Data RAM (DDRAM),
   - Character Generator RAM (CGRAM),
   - Character Generator ROM (CGROM),
   - Chip and Mode Identifier (CMID),
   - Memory access control circuits, address and data multiplexer.
3) **LCD drivers circuit with voltage level shift:**
   - Parallel-to-serial data converter for transfer Character Generator data to SEG shift register,
   - COM counter & decoder,
   - COM drivers,
   - SEG shift register and output latches,
   - SEG drivers,
   - Extension drivers interface.

2. LOGIC CONTROL CIRCUIT

2.1. MPU bus interface

Interface registers

The An6866 has two 8-bit interface registers: instruction register (IR) and data register (DR). Instruction register is write-only and it stores instruction codes. Data register is read/write (write – DRin, read – DRout). Data exchange between registers and MPU perform through bi-directional Data Bus (DB).

Registers are selected by RS signal, and read/write operations are selected by RW signal (refer to table 1).

Table 1 Interface Register selection

RS	RW	Operation
0	0	Writing instructions into IR
0	1	Reading Busy Flag (DB7) and Address Counter (DB6-DB0)
1	0	Writing data into DR
1	1	Reading data from DR

The IR register is used to store instruction code while instruction executing.

The DR register is used for temporary storage of data to be read/write to DDRAM or CGRAM. While executing any instruction RAM data always is read automatically, thus DRout always contains data from the last address (even if the address was changed during instruction execution). This data can be read from DB-bus by the next read instruction. It is guaranteed that MPU always receives data from the last address.

The main function of interface registers is separating MPU interface timing diagram from internal controller timing diagram. IR and DR registers allow to release MPU data bus during instruction execution. While instruction execution, registers are locked, and information in registers can not be changed.

Busy Flag (BF)

Before writing the next instruction, MPU must ensure that previous instruction is completed and interface registers are free. To make this, MPU can check Busy Flag (BF). If BF=1, the controller is executing the previous instruction, and MPU must perform idle cycles or other operations. The next instruction must be written after ensuring that BF is "0".

Busy Flag is read when RS=0 and RW=1 at DB7 pin (see Table 1). Reading BF procedure is used only for checking controller state and it is not an instruction, i.e. it does not lock input registers.

4- and 8-bit interface bus

The An6866 can operate with 4- or 8-bit interface bus. Bus width is selected by DL bit of Function Set instruction (see part 2.10).

- In 8-bit mode (DL=1) all 8 bits are used. Data is strobed by E signal. Instructions start executing at the E fall, and BF sets to "1" (see Fig.2).
- In 4-bit mode (DL=0) only 4 bits (DB4-DB7) are used for exchanging data with MPU. DB0-DB3 bits are not used (pull up to VDD). In 4-bit interface bus mode, instructions and data are transmitted in two passes, corresponding to two E pulses (see figure 3). The four high order bits (DB4 to DB7 for 8-bit operation) are transferred before the four low order bits (DB0 to DB3). Internal data selector multiplexes high and low 4-bit data groups of register, switching at E fall. Instruction writing is complete and BF is set to "1" after the second E pulse. BF must be checked after the second E pulse of instruction.

  Thus, each instruction should be accompanied with strictly two E pulses. If this condition is violated, then the sequence of data following may be broken. In this case the even and the odd 4-bit data groups of the register exchange their places. Single E pulse, owing to MPU synchronization loss or a noise influence, may break all further functioning of the controller.

  To prevent this situation, the controller has the interface synchronization function, which provides the correct order of data following through 4-bit bus: any change of both RS or RW signals resets the selector of the data to the initial status (see figure 3). Also it is forbidden to change RS and RW status during submission of the instruction between E pulses.

2.2. Standard and Extended modes

The An6866 has XMODE pad that allows to control access to some extended functions (see Table 2). The XMODE pad has internal pull up to VDD, therefore, if the XMODE pad is not connected, it has "1" state. The customer may select additional function set for both XMODE states (see part 3.5 "Controller mask option" and Order Form in Appendix 1).

Table 2. Standard and Extended modes

XMODE	Mode	Characteristics
1 or NC*	Standard (compatible)	Mode with standard functions available. Some of Extended functions may be enabled in Standard mode specified by Order Form.
0	Extended	Mode with Extended functions, specified by Order Form : • using of second CGROM page for 5x8 dot characters or 2 pages with software switching, • underline cursor blinking, • display inversion controlling.

*NC-not connected

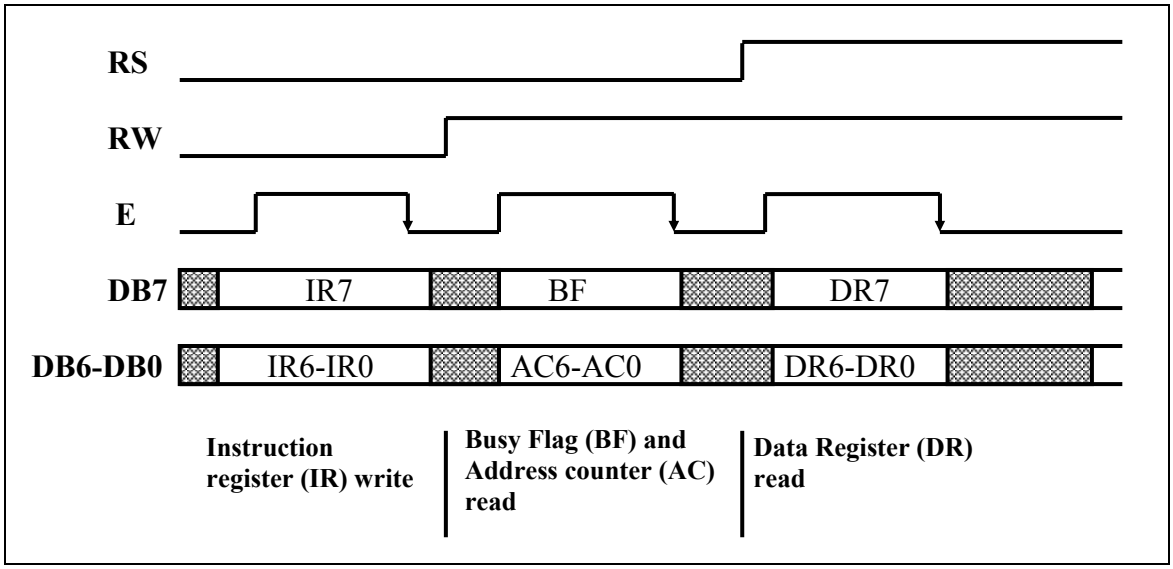
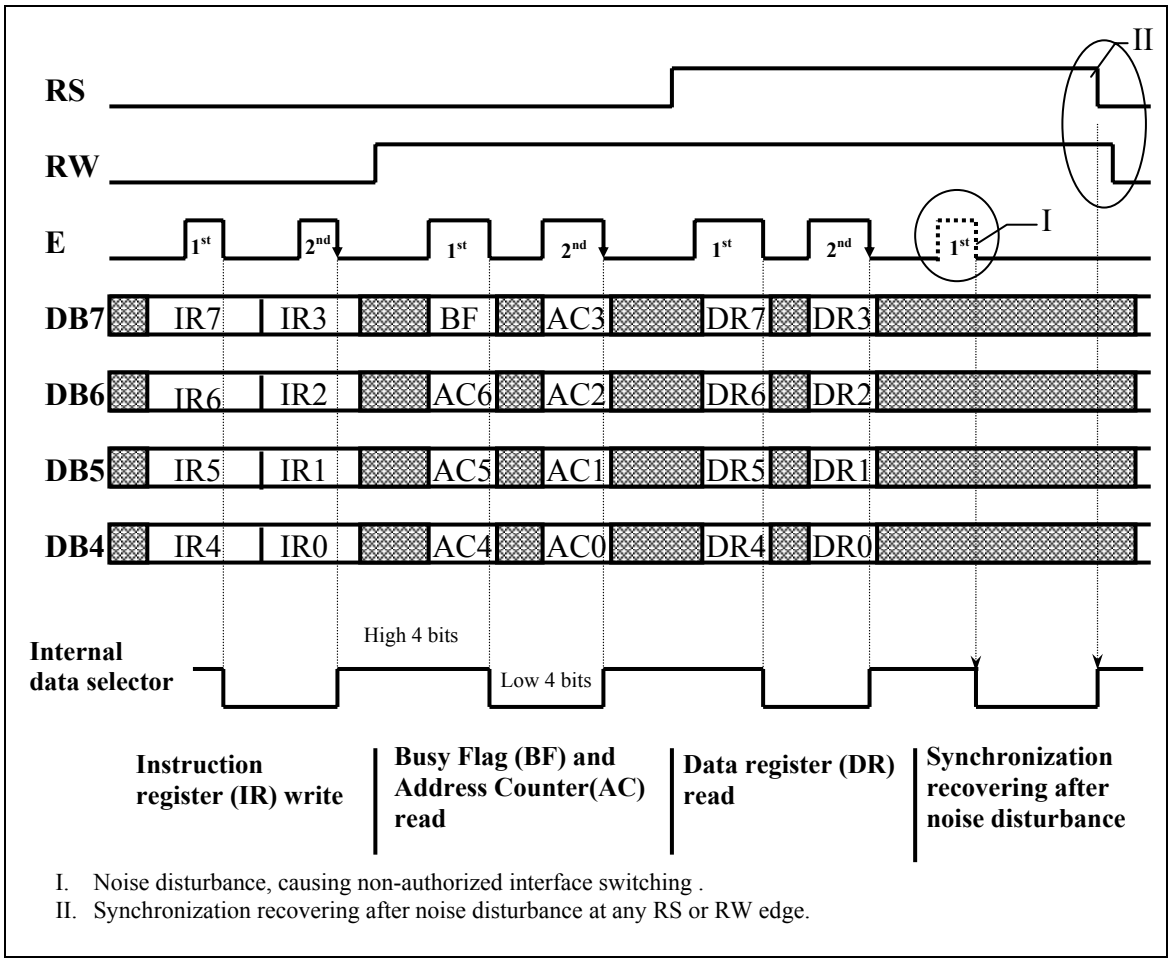


Figure 2. Example of 8-bit interface operation.



I. Noise disturbance, causing non-authorized interface switching .
II. Synchronization recovering after noise disturbance at any RS or RW edge.

Figure 3. Example of 4-bit interface operation.

2.3. One- and two-line display

The controller can display characters in one or two lines. The number of lines is selected by Function Set instruction.

In one-line mode the controller displays characters from single DDRAM address range from 0 to 79 (4Fh). COM[1..8] lines are used for 5x8 dot characters, COM[1..11] lines are used for 5x11 dot characters.

In two-line mode the controller displays characters in two lines accordingly:

- DDRAM address range from 0 to 39 (27h) for the first line (COM[1..8]),
- DDRAM address range from 64 (40h) to 103 (67h) for the second line (COM[9..16]).

Correspondence between DRAM addresses and character positions in one-line mode and an example of cursor displaying in current display position, are shown in Fig. 4, 5.

Correspondence between DRAM address and character positions in two-line mode and example of cursor displaying in current display position, are shown in Fig. 6, 7.

2.4. Address Counter (AC)

The current memory address (DDRAM and CGRAM), and cursor position are determined by Address Counter (AC). AC has reset to 0, setting a given state, increment and decrement functions.

AC resets to 0 when Display Clear and Return Home instructions are executed.

Desired AC value is set by Set DDRAM Address and Set CGRAM Address instructions. In this case the new address value is written into AC from Instruction Register (IR). Selection of memory type (DDRAM or CGRAM) is also made by these instructions.

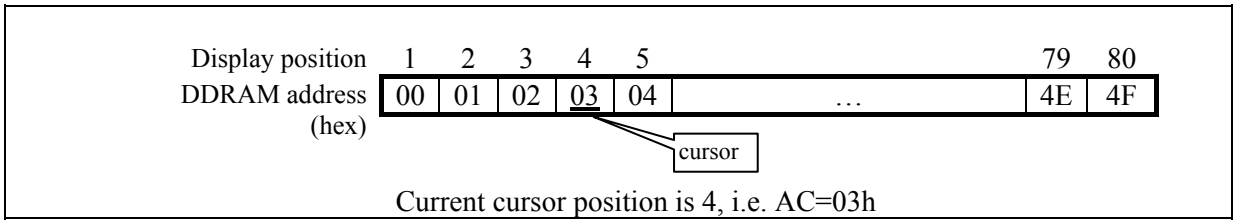


Figure 4. One-line display without shifting.

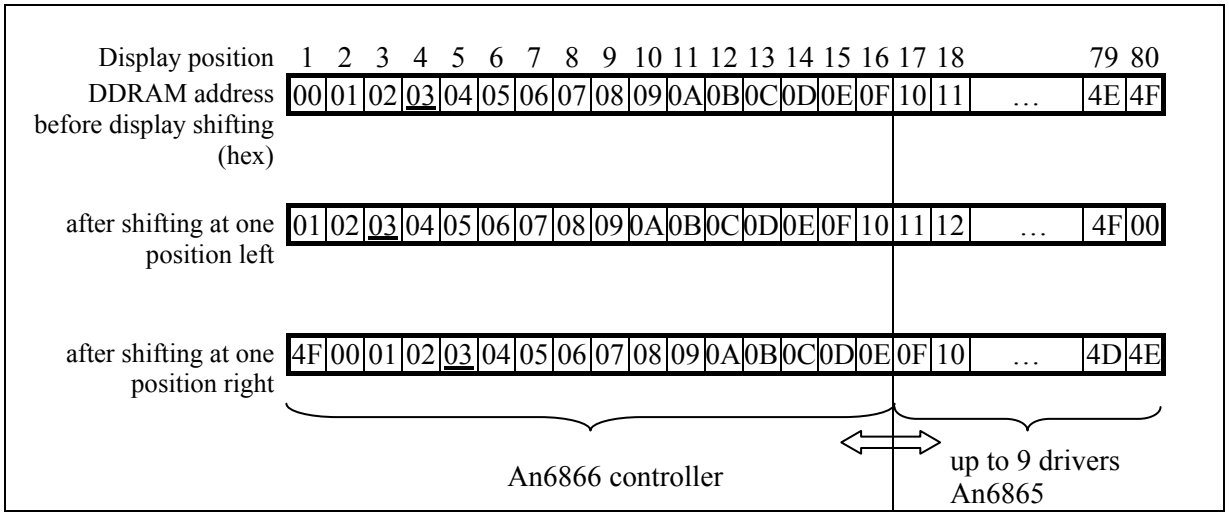


Figure 5. Display shifting in one-line mode.

Incrementing or decrementing of AC address value is made by following instructions:

- Memory read/write operations. Incrementing or decrementing is determined by ID bit of "Set Entry Mode" instruction (see part 2.10 "Instructions description").
- Cursor shift. This instruction also defines shift direction.

Count order of AC is defined by number of display lines (N bit of Function Set instruction) and accessed memory type (DDRAM or CGRAM).

While accessing to CGRAM, AC operates as complete 7-bit reversible counter without limitations (0 to 127). Only 6 bits are used for CGRAM addressing.

While accessing to DDRAM, the count order is following:

- for one-line mode:
  - incrementing: 0, 1, 2, … 78, 79, 0, 1, 2…
  - decrementing: 0, 79, 78, 77, … 2, 1, 0, 79…
  - when AC value more than 79, the counter is incremented to 127 and then sets to 0.
- for two-line mode:
  - incrementing: 0, 1, 2, … 38, 39, 64, 65, … 102, 103, 0, 1, …
  - decrementing: 0, 103, 102, … 65, 64, 39, 38, … 2, 1, 0, 103, …
  - when AC value more than 103, the counter is incremented to 127 and then sets to 0.

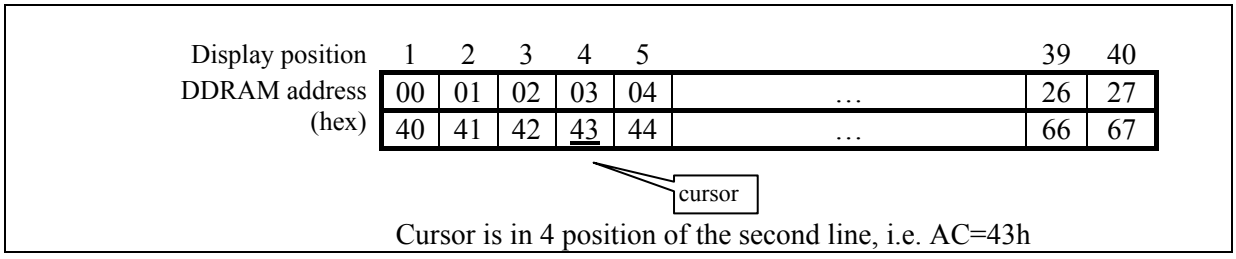


Figure 6. 2-line display without shifting.

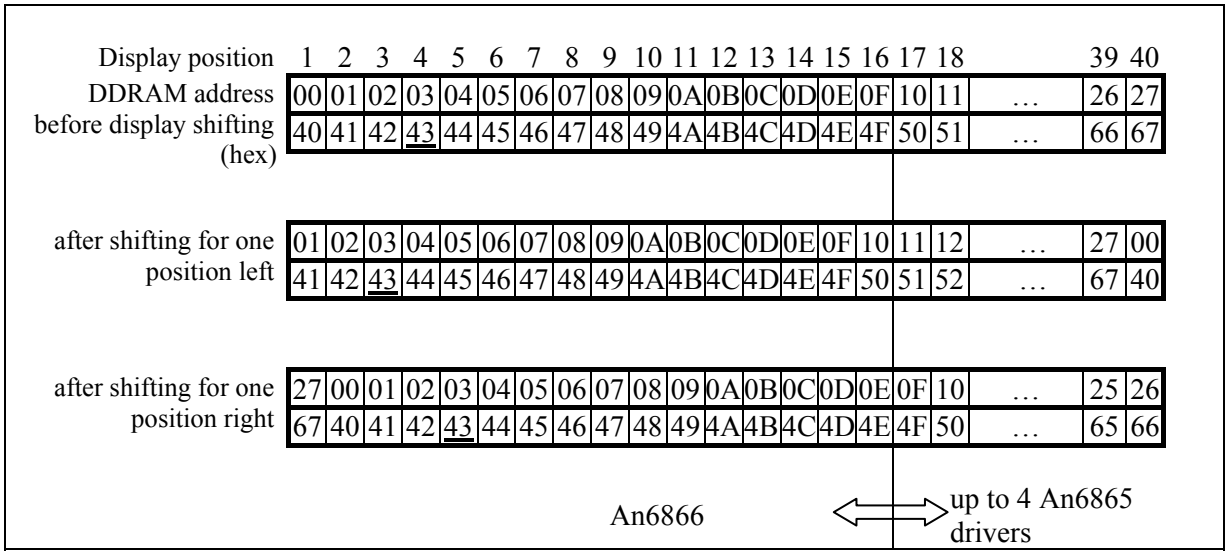


Figure 7. Display shift in 2-line mode.

2.5. Start Address Counter and display shifting

The Start Address Counter is used for display shifting. This counter contain DDRAM address, which is used in the beginning of each COM-line scanning cycle to define the initial value of Refresh Counter. The Start Address Counter has a reset function and incrementing/decrementing functions.

The counter resets to the initial state when instructions Display Clear and Return Home are executed. After resetting, character line is displayed from 0 address of DDRAM.

The counter is incremented or decremented by Display Shift instruction according to shift direction. Count order is the same as for the AC counter (see part 2.4).

The counter has no address set function, and its state is not readable through MPU interface.

Correspondence between DDRAM address and displayed characters positions after left/right display shift in 1-line mode, is shown in Figure 5.

Correspondence between DDRAM address and displayed characters positions after left/right display shift in 2-line mode, is shown in Figure 7.

2.6. Timing Diagram

The internal controller timing diagram consists of periods, each one 5 clocks long. This is the time for transferring one character data (5-bit width) to output SEG register.

Each period contains three sequential phases of timing diagram:

1) phase of writing data to DDRAM/CGRAM and instruction execution,
2) phase of reading data from DDRAM/CGRAM to output data register of MPU interface,
3) phase of reading data from DDRAM/CGRAM/CGROM, and character displaying on the LCD (i.e. display refresh).

This solution provides complete time division between memory access processes, instructions execution, and display refresh. The MPU interface operates only with IR and DR registers with its own frequency independently from the slow controller timing diagram.

Phase 1 (2 clocks) provides MPU instructions execution, including instructions with memory accessing, using the address value stored in the AC. After completing data writing operation, the AC value is incremented or decremented if needed.

Phase 2 (1 clock) serves to read data from DDRAM/CGRAM to output data register DRout. Since the reading phase follows writing and instruction execution phase, data reading always occurs after address changing, if it took place during instruction execution. The following data reading instruction will allow to receive data from MPU interface, and data register will be filled with new data from the next memory address.

Phase 3 (2 clocks) provides display refresh and is used to transfer data from CGRAM/CGROM to the data shift register. The DDRAM character code, CGROM page number, and active COM number are used as CGRAM/CGROM address.

For execution of any instruction (except Display Clear) a complete pass of the 1st and 2nd phases is required. These two phases constitute Instruction Execution time, that is in a range from 3 to 8 clocks (see part 8.2). Display Clear instruction writes sequence of space characters (20h) into all 80 DDRAM addresses, which takes not more than 403 clocks.

There is possibility of express instructions execution under some additional conditions (see part 8.2).

Timing diagram of LCD depends on displaying mode.

In 1-line mode 80 characters of 5 bit wide are displayed, therefore the period of active COM state is 80x5=400 clocks (1.48 ms at Fosc=270 kHz). Display refresh period is:

- for font 5x8 (i.e. 8 active COM lines): 8x1.48=11.84 ms, i.e. frame frequency is ≈84.3 Hz;
- for font 5x11 (i.e. 11 active COM lines): 11x1.48=16.28 ms, i.e. frame frequency is ≈61.4 Hz.

In 2-line mode 40 characters per each line can be displayed, therefore, the time of active COM state is 40x5=200 cycles (0.74 ms at Fosc=270 kHz). Display refresh period is 16x0.74=11.84 ms, i.e. frame frequency is ≈84.3 Hz.

Note that the controller always outputs data for a full character line, but the real number of displayed characters depends on the LCD size and number of connected extension drivers.

The controller timing diagram (except MPU interface) is closured to CLK2 clock grid, that is equal to oscillator frequency F_{OSC}, therefore, the controller timing diagram changes proportionally to F_{OSC} changing.

2.7. Cursor/Character Blink control

The timer-divider with ≈0.76 sec cycle at Fosc=270 kHz is used for cursor/character blinking. Cursor or character blinking position is defined by the AC.

2.8. Power On Reset Function

The internal reset circuit automatically initializes the An6866 when the power is on. BF is kept in the busy state until the initialization is finished. Time needed for reset procedure is up to 12 ms at Fosc=270kHz.

Reset procedure performs the following functions:

- Clear Display;
- Function Set:
  DL=1, 8-bit interface*),
  N=0, 1-line display*),
  F=0, 5x8 dot character format*);
  P=0, Select of the first CGROM page, if software page control is enabled;
  I=0, Inversion is off, if inversion control is enabled;
- Display on/off:
  D=0, Display is off,
  C=0, Cursor is off,
  B=0, Blinking is off;
- Entry Mode Set:
  I/D=1, address increment mode,
  S=0, display shift disable.

*) Note: Initial state of DL, N, F bits of Function Set instruction can be defined by the Customer at the mask option order (see part 3.5. "Controller mask option").

The timer using for the initial reset procedure allows to obtain a stable result at VDD rising time up to 20 ms. However, if electrical characteristics of the device do not satisfy the conditions in part 6.3 "Power on conditions when using internal reset circuit", or if VDD voltage influence occurs, then the reset procedure may fail and cause an initialization error. In this case, it's possible to perform the initialization by instruction (see part 5.1 "Initialization by Instruction").

2.9. Instruction execution

An6866 has only two program accessible registers – instruction register (IR) and data register (DR). The number of register states and two control signals (RW – Read/Write and RS – Register Select) is determined by instruction set (Table 3). The instruction set may be divided into 4 categories:

- determination of the controller operation mode (display format, interface bus width etc.);
- setting the internal memory address and cursor position;
- transferring data between internal memory and MPU;
- service functions executing (Display Clear, Cursor Move etc.).

Usually, most of executing instructions are the data transferring instructions. To speed-up memory loading, the controller has an autoincrement memory address function. At that, the controller can also shift display automatically, which minimizes number of instructions, for example, in case the cursor

reaches the end of display.

For correct controller functioning, before each instruction writing, MPU must ensure that the previous instruction is completed and that interface registers are free. This can be made in two ways:

- By checking Busy Flag until its sets to 0. It is the most efficient way (see Figure 8 and 9).
- By time delay between instruction write, exceeding the maximum previous instruction execution time (see Table 3). It is a simple and slow method, but it is usable when data reading from the controller is never used (RW is fixed to 0). 4-bit interface synchronization function ensures maximum reliability of the controller operation with using only 6 interface lines (DB[7:4], E, RS).

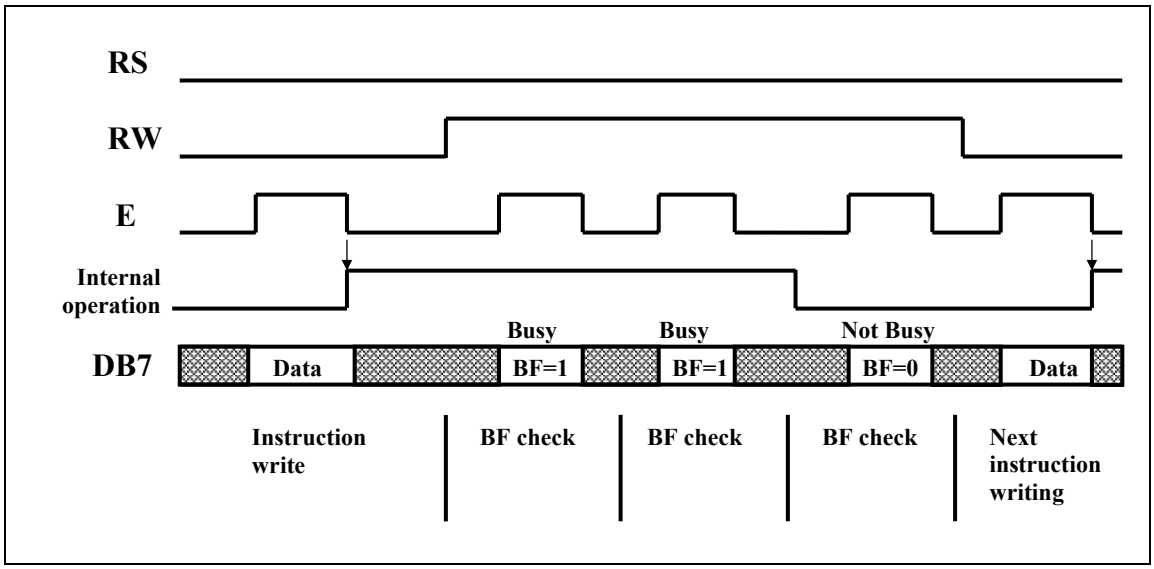


Figure 8. Example of instruction writing with Busy Flag check in 8-bit interface mode.

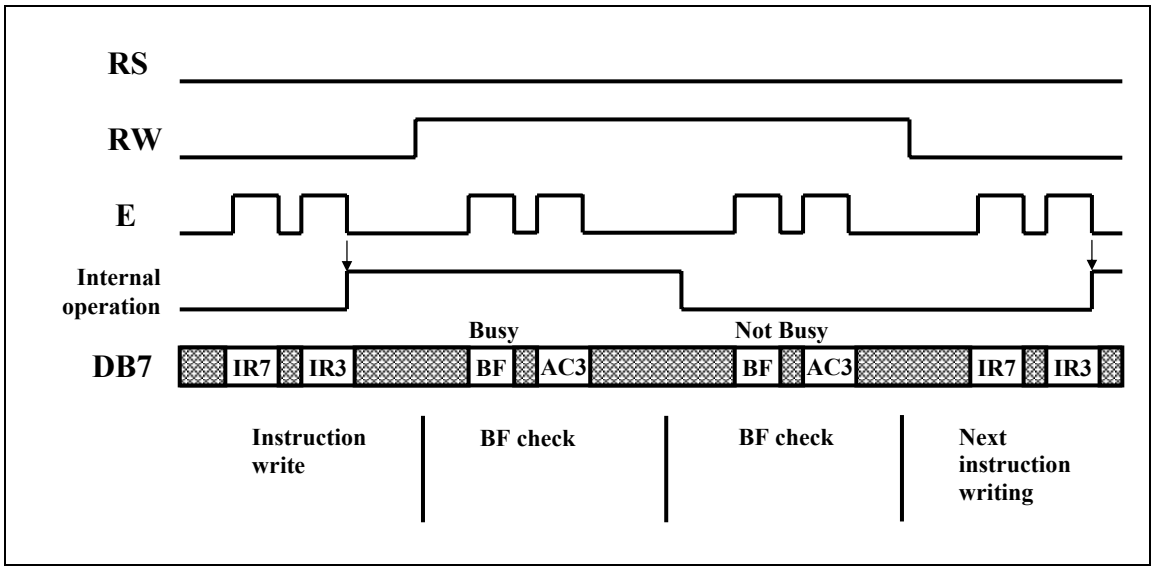


Figure 9. Example of instruction writing with Busy Flag check in 4-bit interface mode.

Table 3. Instructions

Instruction	Code										Description	Max exec. time (Fosc=270 kHz)
	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Display Clear	0	0	0	0	0	0	0	0	0	**1**	Clear entire display and sets DDRAM address 0 in AC.	1,5 ms
Return Home	0	0	0	0	0	0	0	0	**1**	–	Sets AC and Display shift counter to 0. DDRAM contents remain unchanged.	29.6 µs
Entry Mode Set	0	0	0	0	0	0	0	**1**	**I/D**	**S**	Sets cursor move direction and specifies display shift (enables only for writing).	29.6 µs
Display on/off Control	0	0	0	0	0	0	**1**	**D**	**C**	**B**	Sets entire display (D), cursor (C) and blinking of cursor position character (B) on/off.	29.6 µs
Cursor or Display Shift	0	0	0	0	0	**1**	**S/C**	**R/L**	–	–	Moves cursor (C) and shift display (S) without changing DDRAM contents left or right (R/L).	29.6 µs
Function Set	0	0	0	0	**1**	**DL**	**N**	**F**	**P*)**	**I*)**	Set Interface data length (DL), number of display lines (N), character font (F), current page number (P), and inversion mode (I).	29.6 µs
Set CGRAM Address	0	0	0	**1**	**A_{CG}**	**A_{CG}**	**A_{CG}**	**A_{CG}**	**A_{CG}**	**A_{CG}**	Sets CGRAM address. CGRAM data is send and received after this setting.	29.6 µs
Set DDRAM Address	0	0	**1**	**A_{DD}**	**A_{DD}**	**A_{DD}**	**A_{DD}**	**A_{DD}**	**A_{DD}**	**A_{DD}**	Sets DDRAM address. DDRAM data is send and received after this setting.	29.6 µs
Read Busy Flag and Address	0	**1**	**BF**	**AC**	**AC**	**AC**	**AC**	**AC**	**AC**	**AC**	Reads BF and AC. This procedure do not blocking controller interface.	0 µs
Write data to CGRAM or DDRAM	**1**	**0**	**Write data**								Writes data to CGRAM or DDRAM.	29.6 µs
Read data from CGRAM or DDRAM.	**1**	**1**	**Read data**								Reads data from CGRAM or DDRAM.	29.6 µs

I/D: 1- Increment, 0- decrement;
S: 1- display shift enable when write to DDRAM;
D: 1- display is on, 0- display is off;
C: 1- cursor is on, 0- cursor is off;
B: 1- blinking is on, 0- blinking is off;
S/C: 1- Display shift, 0- cursor shift;
R/L: 1- Shift to the right, 0- Shift to the left;
DL: 1- 8-bit interface, 0- 4-bit interface;
N: 1- two-line display, 0- one-line display;
F: 1- font 5x11, 0- font 5x8;
P: 1- Second CGROM page, 0- First CGROM page;
I: 1- Display inversion is on, 0- Display inversion is off;

DDRAM – Display Data RAM.

CGRAM – Character Generator RAM.

A_{CG} – 6-bit CGRAM address.
A_{DD} – 7-bit DDRAM address.
AC – Address Counter for CGRAM and DDRAM addressing.
BF: 1 - Internally operating, 0 - Instructions acceptable.

– indicates no effect.
*) Extended function. Defined by Mask option (version) of controller and XMODE state

2.10. Instructions

Display Clear

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Display Clear writes space code 20h (character pattern for character code 20h must be a blank pattern) into all DDRAM addresses. Then it sets DDRAM address 0 into the address counter, and returns the display to its initial status if it was shifted. In other words, the display disappears and the cursor or blinking goes to the left edge of the display (in the first line if 2 lines are displayed). It also sets I/D bit to 1 (increment mode) in entry mode. S bit of entry mode does not change.

Return Home

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	0

Return Home sets DDRAM address 0 into the Address Counter, and returns the display to its initial status if it was shifted. The DDRAM contents do not change. According to this settings the cursor returns to the initial position, i.e. to the left edge of the display (in the first line if display in the 2-line mode).

Entry Mode Set

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	ID	S

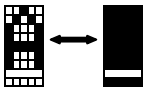
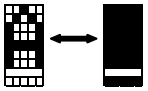
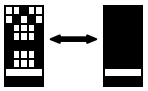
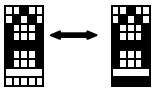
I/D: Incrementing (I/D=1) or decrementing (I/D=0) the DDRAM address by 1 occurs when a character code is written into or read from DDRAM.
The cursor or blinking moves to the right when incremented by 1 and to the left when decremented by 1. The same applies to writing and reading of CGRAM.
S: When the character code is being written to DDRAM, the entire display is shifted either to the right (I/D=0) or to the left (I/D=1) when S is 1. The display does not shift if S is 0.
If S is 1, it will seem as if the cursor does not move but the display does. The display does not shift when reading from DDRAM. Also, writing into or reading out from CGRAM does not shift the display.

Display on/off

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

D: The display is on when D is 1 and off when D is 0. When off, the display data remains in the DDRAM, but can be displayed instantly by setting D to l.
When the display off, the repeating memory access for display refresh is absent and consumption current is decreased.
C: The cursor is displayed when C is 1 and not displayed when C is 0 in position corresponding to the AC. The cursor is displayed using 5 dots in the 8th line for 5x8 dot character font selection and in the 11th line for the 5x11 dot character font selection.
B: The character indicated by the cursor blinks when B is 1.
The cursor blinking mode is an extended function, and its use depends on chip version and XMODE state. For C=1 and B=1 case cursor blinking enable allows to obtain more effective view than character blinking when cursor is permanent on (see Table 4).

Table 4. Cursor displaying and character blinking modes

C	B	Cursor blink disable	Cursor blink enable
0	0	 Cursor is off, blink is off	 Cursor is off, blink is off
0	1	 Cursor is off, character blink	 Cursor is off, character blink
1	0	 Cursor is on, blink is off	 Cursor always on, blink is off
1	1	 Cursor always on, character blink	 Cursor blink

Cursor and Display Shift

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	-	-

Cursor and Display Shift instruction shifts the cursor position or entire display to the right or left without changing DDRAM data (table 5). This function is used to correct or search the display. When display is shifting, cursor position follows to the display move.

In a 2-line display, the cursor moves to the second line when it passes the 40th digit of the first line and vice versa. Note that the first and second display lines shift at the same time. When the display is shifted repeatedly, each line moves only horizontally. The characters in the second display line do not shift into the first line (see Figure 7).

The address counter (AC) contents will not change if the display shift is performed.

Table 5. Cursor and Display Shift modes

S/C	R/L	Description
0	0	Cursor moves left (AC decrement by 1)
0	1	Cursor moves right (AC increment by 1)
1	0	Display shift to left (start address counter increment by 1)
1	1	Display shift to right (start address counter decrement by 1)

Function Set

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	F	P	I

DL: Sets the interface data length. Data is transferred in 8-bit lengths (DB7-DB0) when DL=1, and in 4-bit lengths (DB7-DB4) when DL=0. When 4-bit length is selected, data must be transferred in two passes.

N: Sets the number of display lines.

F: Sets the character font.

Table 6. Function set modes

N	F	Display lines	Font size	Duty cycle	Notes
0	0	1	5x8	1/8	
0	1	1	5x11	1/11	
1	*	2	5x8	1/16	displaying 2 lines of 5x11 characters is impossible.

* -no effect.

P: Select of CGROM page: P=0 – the first page, P=1 – the second page. P bit allows to select CGROM page in the An6870 with the software support.

Two CGROM pages is an extended function in the An6866 controller. Possibility of the second page selection depends on chip version and XMODE state.

The following second CGROM page selections are possible:

- the second page is disabled, access to the first page at any case;
- page selection only by XMODE signal (fixed pages). In the standard mode the first page is selected by default (XMODE=1), in the extended mode (XMODE=0) the second page is selected. Software page selection is disabled, P bit has no effect;
- In the standard and/or extended mode software page selection is enabled, which allows to extend system functionality with MPU software support.

I: Display inversion on/off. At I=1 black pixels become white (transparent). Inversion mode with back lighting allows to obtain "Information Board" view with bright characters on the black (dark) background.

Display inversion is an extended function, and its use depends on chip version and XMODE state.

The main features of Display Inversion function are the same as for Page Selection function (see above): disable, switching on/off by XMODE signal or software control.

Set CGRAM address

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC[5]	AC[4]	AC[3]	AC[2]	AC[1]	AC[0]
				MSB					**LSB**

Set CGRAM address instruction writes 6-bit CGRAM address into the AC. After this instruction execution CGRAM is set as memory for reading/writing data.

Set DDRAM address

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	AC[6]	AC[5]	AC[4]	AC[3]	AC[2]	AC[1]	AC[0]
			MSB						**LSB**

The instruction Sets 7-bits DDRAM address into the AC. After this instruction execution DDRAM is set as memory for reading/writing data.

In 1-line mode (N=0) DDRAM address AC[6..0] must be in 00h-4Fh (0-79) range. In 2-line mode (N=1) DDRAM address AC[6..0] must be in 00h-27h (0-39) range for the first line and in 40h-67h (64-103) range for the second line.

CMID can be found in DDRAM address range 78h-7Fh (120-127, see part 3.4).

Read Busy Flag and Address

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BF	AC[6]	AC[5]	AC[4]	AC[3]	AC[2]	AC[1]	AC[0]
			MSB						**LSB**

Read Busy Flag and Address instruction reads the BF indicating that the system is now internally executing the previous instruction. If BF=1, the internal operation is in process. The next instruction will not be accepted until BF is reset to 0. MPU must check the BF status before writing the next instruction. Simultaneously AC value at DB6-DB0 can be read by MPU. The address format is the same as for Set CGRAM/DDRAM Address instructions.

Note, that the AC can change during execution (i.e. BF=1) of some instructions, such as data read/write, cursor move etc. It is impossible to fix the moment of AC change relatively to E fall, but it has a fixed time interval till changing BF state to 0. This interval can be used for accurate estimation of oscillator frequency (see part 8.4). Read BF procedure is used only to determine the controller status and it is not an instruction, because it does not change the controller state (executing time is 0).

Write Data to CGRAM or DDRAM

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
		MSB							**LSB**

The Write Data to CGRAM or DDRAM instruction writes 8-bit binary data to CGRAM or DDRAM.

The Address is determined by the previous specification of the CGRAM or DDRAM address setting. After a write, the address is automatically incremented or decremented by 1 according to the I/D bit of entry mode. Also it is possible to shift entire display backward when data writing to DDRAM (not CGRAM!), if this operation enabled by S bit of entry mode.

Read Data from CGRAM or DDRAM

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
		MSB							**LSB**

The Read Data from CGRAM or DDRAM instruction reads 8-bit binary data D[7..0] from CGRAM or DDRAM at AC address into data bus interface.

Reading data from DDRAM/CGRAM is realized in two stages. First, after any instruction execution CGRAM/DDRAM data is put into output data register (DRout). This is guaranteed that data in the DRout is always from the last address, even if it has been changed during the last instruction execution. At high E level data from the DRout is transferred to data bus interface. Then at E fall the controller performs AC incrementing or decrementing during instruction execution according to I/D bit of entry mode. At that, reading data from next memory address into DRout is performed.

Automatical AC incrementing or decrementing imply that the last writed data cannot be verified immediately by the Read instruction. If the verification is needed, executing the address set or cursor move instructions must be performed before reading data.

When data reading, the display is not shifting.

3. INTERNAL CONTROLLER MEMORY

3.1. Display Data RAM (DDRAM)

DDRAM stores display data represented in 8-bit character codes.

In read/write mode, access to DDRAM is made at the current AC address. DDRAM addressing depends on the number of display lines:

- in 1-line mode address, range from 0 to 79 is used,
- in 2-line mode, the following address ranges are used (see part 2.4):
  - 0-39 for the first line,
  - 64-103 for the second line.

At display refresh, the code read from the DDRAM combined with the current COM number and page number is used to generate CGROM/CGRAM address. Character pattern information from CGROM/CGRAM is used for displaying characters on LCD.

3.2. Character Generator ROM (CGROM)

CGROM pattern is programmed by mask option during manufacture. There are 2 available font sizes: 5x8 and 5x11 dots.

8-bit character code allows to display simultaneously up to 256 characters from the character pattern table (see Appendix 3). Each character code is composed from 4-bit column address and 4-bit row address. 240 or 248 codes may be assigned to the CGROM, correspondingly 16 or 8 codes remain for the CGRAM.

The CGROM consists of 248 character cells of 5x16 size. In each cell it is possible to place two 5x8 dot characters or one 5x11 dot character. The 5x8 dot character set forms two CGROM pages, accessible by P bit of Function Set instruction and XMODE signal (depends on the controller mask option). 5x11 dot characters can not be coded in two pages, therefore, they have only one set and they are displayed equally for both pages.

There are some differences in address generating for 5x8 dot and 5x11 dot characters (see tables 7 and 8). Therefore, the controller contains special circuits - comparators of 4 high order bits of the address that defines code range for two-page table region with 5x8 characters: Amin ÷ Amax.

Inside the Amin÷Amax range it is possible to select 5x8 character with P bit (page number) and XMODE state. Outside the Amin÷Amax range it is possible to select characters only from one page, which allows to code one set of 5x8 or 5x11 characters.

Since only 4 high order bits of the address (or character code) are compared, the table may be divided into one-page and two-page parts, multiplicity equals strictly 16 (entire column). For example, for S00 coding Amin=1h and Amax=Dh, which allows to code 208 5x8 characters per each of two pages (10h-DFh), and 32 5x11 characters (E0h-FFh).

For the Customer's new mask option and page control possibilities see part 3.5 "Controller mask option", for released options see Appendix 3.

Note, that in 1-line mode with 1/8 duty (N=0 и F=0), and in 2-line mode, 5x11 dot characters are displayed in a truncated form: only 8 upper COM-lines are displayed. On the other hand, in 1/11 duty mode (i.e. at 11 active COM-lines) 5x8 characters at two-page coding are supplemented with spaces in 9, 10 and 11 COM-lines, thus, providing correct displaying though character presence on the next page (see Table 8).

The An6866 also has a capability to readdress 08h-0Fh codes to CGROM, which is assigned for replication of 00h-07h CGRAM codes. The corresponding function is enabled by the controller mask option according to the Customer's request (see part 3.5). In this case, maximum CGROM capacity is up to 248 characters at each of two pages, 496 characters in two pages in 08h-FFh code range.

3.3. Character Generator RAM (CGRAM)

User can write into CGRAM his own character patterns: 8 characters 5x8 dots or 4 characters 5x11 dots. Correspondence of CGRAM addresses and character codes is shown in Table 9 for 5x8 dots characters and in Table 10 for 5x11 dot characters.

A CGRAM cell, which contains information about one 5x8 character occupies 8 bytes. Every byte contains information about one character line; only 5 low order bits (D4-D0) are used for displaying, 3 high order bits (D7-D5) are not used. CGRAM size is 64 bytes; it is possible to write 8 characters 5x8 dots.

When writing 5x11 characters, each character occupies two 8-byte CGRAM cells. In the second cell 9, 10, 11 character lines are coded. Information in the next 5 bytes is not displayed and may contain general purpose data. CGRAM 5x11 dot character codes will be numbered every other one in 00h-07h code range. For example, if the first character is written in CGRAM from cell 0 occupying cells 0 and 1, it is possible to use codes 00h, 02h, 04h and 06h to display such 4 characters.

Note: When using 5x11 font mode, 5x8 characters must also be coded in 11 lines with spaces in 9, 10, and 11 character lines, because function of automatical space filling, used in 2-page CGROM code table, does not work with CGRAM.

In the standard chip version 16 codes are used for CGRAM. CGRAM characters repeat twice – for codes 00h-07h and 08h-0Ah. At that, the D3 bit of character code is not used for CGRAM addressing.

For advanced possibilities, the D3 bit (address A7, see Table 9) may be used for CGROM/CGRAM address sharing. Codes 00h-07h remain for CGRAM. 8 additional codes (08h-0Fh) pass to CGROM, thus, increasing the total character numbers up to 248.

In Tables 9 and 10 there are complete addresses used to address CGROM/CGRAM, and corresponding AC addresses used for access through the MPU interface.

Table 7. CGROM addressing and 5x8 dot character coding

CGROM Address												Data					
Character code								P	COM[1..8]								
A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Q_4	Q_3	Q_2	Q_1	Q_0	
								0	0	0	0	**1**	0	0	0	0	
								0	0	0	1	**1**	0	0	0	0	
								0	0	1	0	**1**	0	**1**	**1**	0	
								0	0	1	1	**1**	**1**	0	0	**1**	**First page**
								0	1	0	0	**1**	0	0	0	**1**	
								0	1	0	1	**1**	0	0	0	**1**	
								0	1	1	0	**1**	**1**	**1**	**1**	0	
0	1	1	0	0	0	1	0	0	1	1	1	0	0	0	0	0	← cursor position
								1	0	0	0	**1**	0	0	0	0	
								1	0	0	1	**1**	0	0	0	0	
								1	0	1	0	**1**	**1**	**1**	**1**	0	
								1	0	1	1	**1**	0	0	0	**1**	**Second page**
								1	1	0	0	**1**	0	0	0	**1**	
								1	1	0	1	**1**	0	0	0	**1**	
								1	1	1	0	**1**	**1**	**1**	**1**	0	
								1	1	1	1	0	0	0	0	0	← cursor position

Notes:
1. Character code, corresponding to the addresses A_{11}-A_4, is chosen from DDRAM (D7-D0) according to the character position on the display.
2. P (address A_3) –CGROM page number.
3. Addresses A_2-A_0 –COM[1..8]-line number.
4. Pixel is "on" corresponding to "1" in CGROM.

Table 8. CGROM addressing and 5x11 dot character coding

CGROM Address												Data					
Character code								COM[1..11]									
A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Q_4	Q_3	Q_2	Q_1	Q_0	
								0	0	0	0	**1**	0	0	0	0	
								0	0	0	1	**1**	0	0	0	0	
								0	0	1	0	**1**	0	**1**	**1**	0	
								0	0	1	1	**1**	**1**	0	0	**1**	**First page**
								0	1	0	0	**1**	0	0	0	**1**	**or**
								0	1	0	1	**1**	0	0	0	**1**	**Second page**
								0	1	1	0	**1**	**1**	**1**	**1**	0	
0	1	1	0	0	0	1	0	0	1	1	1	0	0	0	0	0	
								1	0	0	0	0	0	0	0	0	At 1/11duty 5x8 character is supplemeted with "0" in 9, 10 and 11 lines
								1	0	0	1	0	0	0	0	0	
								1	0	1	0	0	0	0	0	0	←cursor position
								1	0	1	1	*	*	*	*	*	
								1	1	0	0	*	*	*	*	*	
								1	1	0	1	*	*	*	*	*	
								1	1	1	0	*	*	*	*	*	
								1	1	1	1	*	*	*	*	*	
…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	
								0	0	0	0	0	0	0	0	0	
								0	0	0	1	0	0	0	0	0	
								0	0	1	0	0	**1**	**1**	0	**1**	
								0	0	1	1	**1**		0	**1**	**1**	
								0	1	0	0	**1**	0	0	0	**1**	
								0	1	0	1	**1**	0	0	0	**1**	
								0	1	1	0	0	**1**	**1**	**1**	**1**	
1	1	1	1	0	0	0	1	0	1	1	1	0	0	0	0	**1**	
								1	0	0	0	0	0	0	0	**1**	
								1	0	0	1	0	0	0	0	**1**	
								1	0	1	0	0	0	0	0	0	←Cursor position
								1	0	1	1	*	*	*	*	*	
								1	1	0	0	*	*	*	*	*	
								1	1	0	1	*	*	*	*	*	
								1	1	1	0	*	*	*	*	*	
								1	1	1	1	*	*	*	*	*	

Notes:
1. Character code, corresponding to the addresses A_{11}-A_4, is chosen from DDRAM (D7-D0) according to the character position on the display.
2. Addresses A_3-A_0 – COM[1..11]-line number.
3. 5x8 characters from two-page area (Amin÷Amax) are supplemented with "0" in COM[9..11]-lines.
4. Characters from one-page area out of the address range (Amin÷Amax) occupy all 11 lines.
5. Data in COM[12..16]-lines are not displayed (sign *).
6. Pixel is "on" corresponding to "1" in CGROM.

Table 9. CGRAM addressing for 5x8 dot characters

CGRAM selection sign					CGRAM Address								Data								
Character code								COM[1..8]													
					AC_5	AC_4	AC_3		AC_2	AC_1	AC_0		MSB							LSB	
A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	
								*	0	0	0		*	*	*	**1**	**1**	**1**	**1**	0	
								*	0	0	1		*	*	*	**1**	0	0	0	**1**	
								*	0	1	0		*	*	*	**1**	0	0	0	**1**	
								*	0	1	1		*	*	*	**1**	**1**	**1**	**1**	0	**First**
0	0	0	0	*	0	0	0	*	1	0	0		*	*	*	**1**	0	**1**	0	0	**character**
								*	0	0	1		*	*	*	**1**	0	0	**1**	0	
								*	1	0	0		*	*	*	**1**	0	0	0	**1**	
								*	1	0	1		*	*	*	0	0	0	0	0	← cursor position
								*	0	0	0		*	*	*	**1**	0	0	0	**1**	
								*	0	0	1		*	*	*	0	**1**	0	**1**	0	
								*	1	0	0		*	*	*	**1**	**1**	**1**	**1**	**1**	
								*	1	0	1		*	*	*	0	0	**1**	0	0	**Second**
0	0	0	0	*	0	0	1	*	0	0	0		*	*	*	**1**	**1**	**1**	**1**	**1**	**character**
								*	0	0	1		*	*	*	0	0	**1**	0	0	
								*	0	1	0		*	*	*	0	0	**1**	0	0	
								*	0	1	1		*	*	*	0	0	0	0	0	← cursor position
…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…

Notes:
1. Character code, corresponding to the address A_{11}-A_4, is chosen from DDRAM (D7-D0) according to the character position on the display.
2. Addresses A_{11}-A_7 indicate CGRAM selection for display refresh (A_{11}-A_7=0000*). Address A_7 is not usually used, that means selection of CGRAM for codes 00h-0Fh. However, it may be additionally determined, at that, A_7=0 will mean selection of CGRAM (8 codes 00h-07h), A_7=1 – selection of CGROM (8 additional codes 08h-0Fh, totally 248 CGROM characters).
3. Addresses A_6-A_4 – CGRAM character code (3 addresses, 8 characters 5x8).
4. Address A_3 – not used to display 5x8 characters.
5. Addresses A_2-A_0 – COM[1..8]-line number.
6. AC_5-AC_0 – the address counter (AC) bits while read/write data operations.
7. Pixel is "on" corresponding to "1" in CGROM.
8. CGRAM Q_7-Q_5 lines are not displayed and can be used as conventional memory.

Table 10. CGRAM addressing for 5x11 dot characters

CGRAM selection sign					CGRAM Address										Data								
Character code								COM[1..11]															
					AC_5	AC_4		AC_3	AC_2	AC_1	AC_0	MSB								LSB	
A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	
0	0	0	0	*	0	0	*	0	0	0	0	*	*	*	0	0	0	0	0	
								0	0	0	1	*	*	*	0	0	0	0	0	
								0	0	1	0	*	*	*	**1**	0	**1**	**1**	0	
								0	0	1	1	*	*	*	**1**	**1**	0	0	**1**	**First character**
								0	1	0	0	*	*	*	**1**	0	0	0	**1**	
								0	0	0	1	*	*	*	**1**	0	0	0	**1**	
								0	1	0	0	*	*	*	**1**	**1**	**1**	**1**	0	
								0	1	0	1	*	*	*	**1**	0	0	0	0	
								1	0	0	0	*	*	*	**1**	0	0	0	0	
								1	0	0	1	*	*	*	**1**	0	0	0	0	
								1	1	0	0	*	*	*	0	0	0	0	0	← cursor position
								1	1	0	1	*	*	*	*	*	*	*	*	
								1	0	0	0	*	*	*	*	*	*	*	*	
								1	0	0	1	*	*	*	*	*	*	*	*	
								1	0	1	0	*	*	*	*	*	*	*	*	
								1	0	1	1	*	*	*	*	*	*	*	*	
0	0	0	0	*	0	1	*	0	0	0	0	*	*	*	0	0	0	**1**	0	
								0	0	0	1	*	*	*	0	0	0	0	0	
								0	0	1	0	*	*	*	0	0	**1**	**1**	0	
								0	0	1	1	*	*	*	0	0	0	**1**	0	**Second character**
								0	1	0	0	*	*	*	0	0	0	**1**	0	
								0	0	0	1	*	*	*	0	0	0	**1**	0	
								0	1	0	0	*	*	*	0	0	0	**1**	0	
								0	1	0	1	*	*	*	0	0	0	**1**	0	
								1	0	0	0	*	*	*	**1**	0	0	**1**	0	
								1	0	0	1	*	*	*	0	**1**	**1**	0	0	
								1	1	0	0	*	*	*	0	0	0	0	0	← cursor position
								1	1	0	1	*	*	*	*	*	*	*	*	
								1	0	0	0	*	*	*	*	*	*	*	*	
								1	0	0	1	*	*	*	*	*	*	*	*	
								1	0	1	0	*	*	*	*	*	*	*	*	
								1	0	1	1	*	*	*	*	*	*	*	*	
…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…

Notes:
1. Character code, corresponding with addresses A_{11}-A_4, is chosen from DDRAM (D7-D0) according to character position on display.
2. Addresses A_{11}-A_7 are indicating selection of CGRAM for display refresh (A_{11}-A_7=0000*). Address A_7 usually not used, that means selection of CGRAM for codes 00h-0Fh. However, it may be additional determined, A_7=0 is mean selection of CGRAM (4 codes from 00h-07h range every other one), A_7=1 – selection of CGROM (additional 8 codes 08h-0Fh, 248 CGROM characters at all).
3. Addresses A_6-A_5 – CGRAM character code (2 addresses, 4 characters 5x11).
4. Address A_4 – not used for display 5x11 characters.
5. Addresses A_3-A_0 –COM[1..11]-line number.
6. AC_5-AC_0 –address counter (AC) bits while read/write data.
7. Pixel is "on" corresponding to "1" in CGROM.
8. CGRAM Q_7-Q_5 lines and bytes 12 to 16 for each character are not displayed and can be used as conventional memory.

3.4. Chip and Mode Identifier (CMID)

The chip version and the current operation mode identifier (Chip & Mode IDentifier - CMID) gives MPU the information about the controller type being used, its functionality, CGROM mask option, the current status and operation mode. The identifier occupies a range of DDRAM addresses from 78h up to 7Fh (120-127). To read all the bits of CMID, it is necessary to set DDRAM address to 78h in the increment mode or 7Fh in the decrement mode and to read sequently 8 bytes of data. The structure of the identifier is given in table 11. Coding variants of the registered controller versions see in Appendix 6.

According to the type of information, the identifier may be divided into two parts: permanent and variable. For the permanent part mask programming is performed at the factory. The mask contains the

Table 11. CMID bits description

Address		An6866 Identificator coding								Parameter
Dec.	Hex.	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
120	78h	0	1	0	0	0	0	0	1	An6866 Chip Identifier
121	79h	0	1	0	0	1	1	1	0	
122	7Ah	0	1	0	0	0	1	0	0	
123	7Bh	0	1	0	0	0	0	1	0	
124	7Ch	PF	V	V	V	V	V	V	V	CGROM mask
125	7Dh	NL	NF	FS	FF	PN	PX	IN	IX	Configuration
126	7Eh	0	SZ	CBN	CBX	WFN	WFX	P	I	Config./Current state
127	7Fh	X	N	F	D	C	B	ID	S	Current state

Permanent part

V	CGROM characters pattern version
PF	Pages Fix mode (when 1: PN - page number for Standard mode, PX - page number for Extended mode)
NL	Number of Lines
NF	Number of Lines Fix/init
FS	Font Size (5x8 or 5x11)
FF	Font size Fix/init
PN	When PF=1 – page number in Standard mode, When PF=0 – page control enable in Standard mode
PX	When PF=1 – page number in Extended mode, When PF=0 – page control enable in Extended mode
IN	Inverse enable in Standard mode
IX	Inverse enable in Extended mode
SZ	CGROM Size: 1 for double size (for further development)
CBN	Cursor Blink in Standard mode
CBX	Cursor Blink in Extended mode
WFN	WaveForm type in Standard mode (0- A-type, 1- B-type)
WFX	WaveForm type in Extended mode (0- A-type, 1- B-type)

Variable part

P	current page	D	Display on/off
I	current display inversion mode	C	Cursor on/off
X	XMODE state	B	Blinking on/off
N	number of display lines	ID	Address Inc. or Dec. when data read/write
F	font size	S	Display shift enable when write to DDRAM

chip identifier, number of CGROM mask option and flags describing availability of various extended functions in the standard and extended operation modes. The variable part indicates the information on the current software controlled operation modes established by MPU instructions.

Information given by the identifier may be used by MPU software to increase its flexibility and reliability. It is very crucial in mass production of devices with mask ROM MPU. Subject to the controller version, it is possible to use one program placed in MPU ROM to produce devices with different functionalities or for the different markets (countries).

There are some typical ways of the identifier application:

- use controller type data to adjust the program to specified chip features and to distinguish the controller from analogues of other manufacturers;
- use ROM mask option data to solve language problems during the device localization in different markets (countries);
- use controller functional possibilities data for its correct use, also in combination with other functional parts of the device;
- use information of the current controller operation mode to increase total reliability of the device operation, and also for its testing and self-diagnostic.

It is supposed that this access method and identifiers will remain for all chips of dot matrix character controllers family.

3.5. Controller mask option

There are two parts in controller mask option:

- Functional mask option;
- Character Generator ROM mask.

Functional mask option allows to enable or disable extended functions in the standard (XMODE=1) and extended (XMODE=0) modes. A full list of extended functions and comments is given in Order Form (see Appendix 1).

CGROM mask options contains:

- coding of the first and the second CGROM pages,
- address range for the second page (Amin-Amax),
- 08h-0Fh code range CGROM selection enabling.

The Customer specifies all the desired functions in the Order Form (Appendix 1) and his own character code tables (Appendix 3), if needed. All the mask options are programmed by metal layer.

Mask options have unique 4-digit number used in complete controller marking – An6866-xxyy. The first two digits – functional mask version, the last two digits – CGROM version. The version number is designated by ANGSTREM during the customer mask generation.

3.6. Mask option order

The order of new controller mask option is made in the following sequence:

1. The CUSTOMER develops the mask option specification and CGROM character table with help of CGROM font editor program, fills in the Order Form and sends them to ANGSTREM.
2. ANGSTREM checks correctness of the received specification, designates a 4-digit number to the new mask option, develops the appropriate coding of the controller identifier (CMID) and enters the new coding in the CAD system database.
3. ANGSTREM sends to the CUSTOMER the specification of mask option and the CGROM character table, obtained by the CAD system.
4. The CUSTOMER checks conformity of mask option parameters to his requirements and confirms their correctness.
5. ANGSTREM makes an experimental lot and send it to the CUSTOMER to test as a part of user device.
6. After receipt of the positive conclusion from the CUSTOMER, ANGSTREM begins mass production of the controller with the new mask option.

4. LCD DRIVERS CIRCUIT

4.1. LCD interface

The LCD is a matrix consisting of lines (rows) and columns on which crossings there are active elements. Matrix rows are connected to COM [1:16] outputs, and columns - to SEG outputs of controller or extension drivers.

To display information, the multiplexing method is used, i.e. dynamic sharing of the displayed information in time. In every moment of time, information established on the controller SEG outputs is highlighted only for one active COM-line. After a time period equal to the period of line frequency, the next COM becomes active, and the appropriate information is established in SEG outputs for this COM. During the full screen refresh (frame frequency period) all COM-lines are activated according to the duty cycle. It is supposed, that the established pixels status is kept at least for one period of screen update.

The controller can output three types of timing diagram: 1/8, 1/11, 1/16 duty cycle depending on the display mode (see Table 12). The denominator shows the amount of active COM-lines. Other COM-lines always remain passive, and the connected pixels – not highlighted.

Activity of COM-lines is determined by the counter-decoder which sequentially touches all COM-lines up to the maximal value determined by the appropriate display mode.

Information about displaying characters is sent to the controller SEG outputs and extension drivers outputs. The An6866 has positive display logic when "1" corresponds to the highlighted pixel located on the current active COM-line.

Examples of various LCD connection variants are given in Figures 10-14.

Table 12 Display modes

Number of lines	Font size	Number of active COM-lines	Duty cycle
1	5x8	8	1/8
1	5x11	11	1/11
2	5x8	16	1/16

4.2. CGROM output data writing to SEG shift registers

CGROM output data intended for displaying are converted from parallel to serial form and then written into the SEG shift register with CLK2 frequency equal to oscillastor frequency F_{OSC}.

The information about displayed characters is transferred into the shift register in the reverse order, i.e. for each COM-line first the data for the last character are transferred, then the refresh address decreases and the information for the previous character is transferred etc. (for example, see Figure 3 and 4 for one-line mode and Figure 5 and 6 for two-line mode). The number of the last character of the line, which is first loaded into the shift register, is set by the start address counter (see part 2.5 "Start Address Counter and display shifting"). The first 8 characters of a line are always displayed with the own SEG drivers (totally 40 SEG outputs). Data for these characters are received at the end of a COM-line update cycle.

After filling the shift register with the data for the next COM-line, data are written in SEG latches at CLK1 fall, and displayed onto LCD simultaneously with switching to the next COM. Then the shift register fills up with data for the next COM. Thus, a CLK1 pulse is a line frequency synchronization signal.

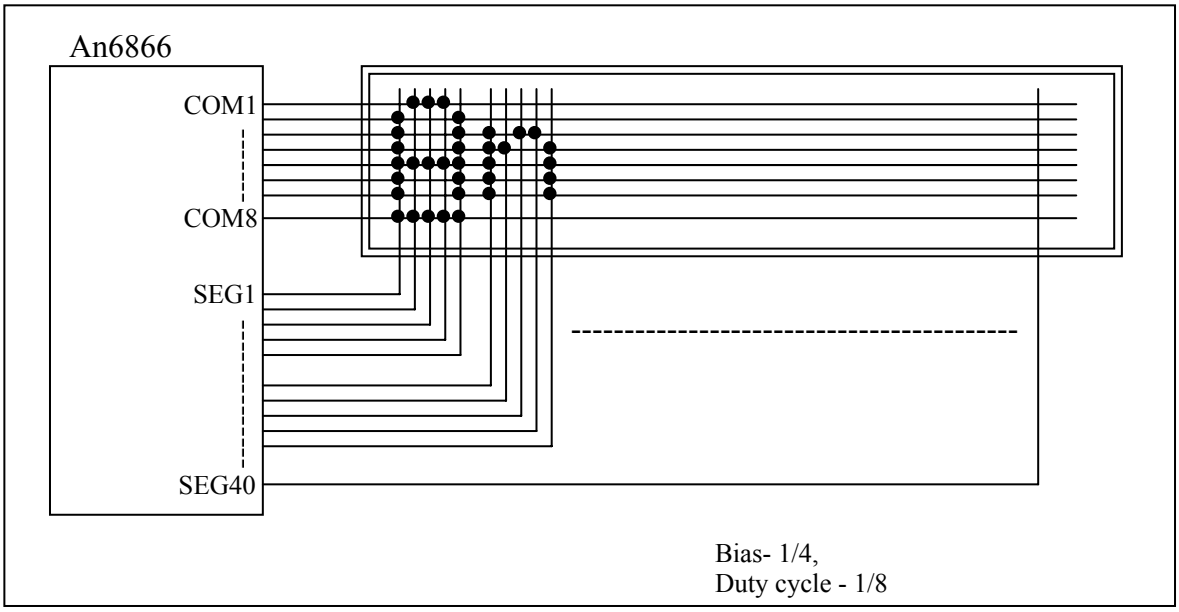


Figure 10. Example of 5x8 dots, 8 character x 1 line display.

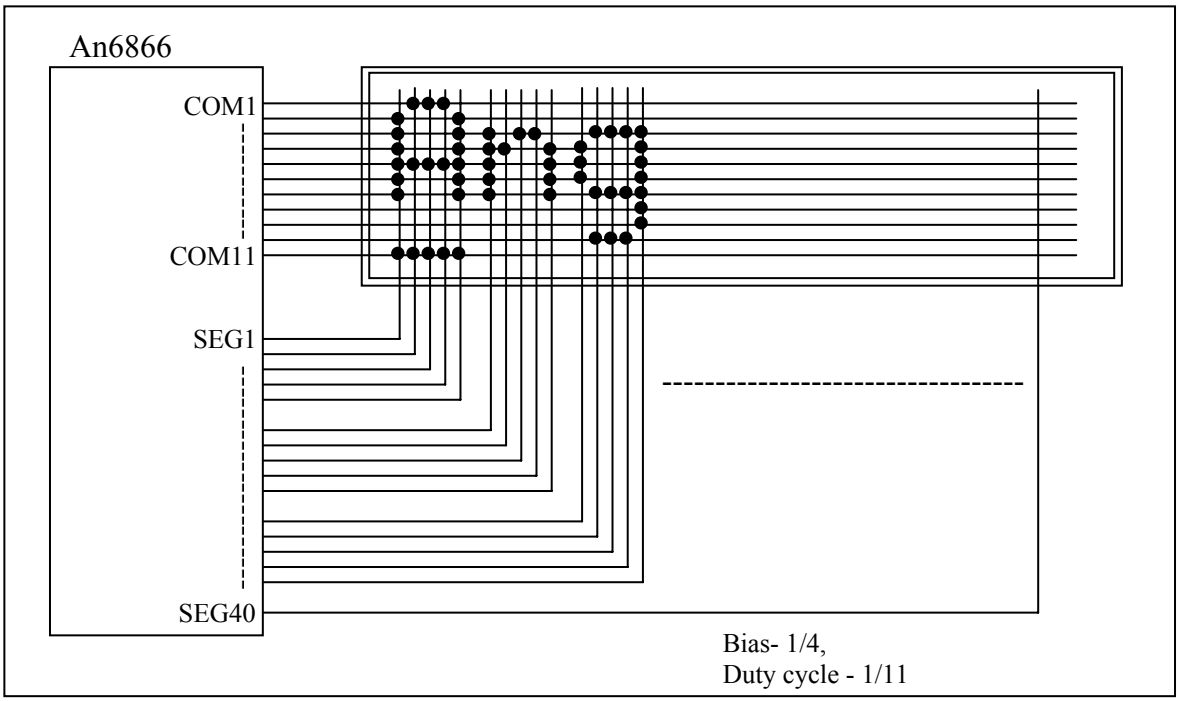


Figure 11. Example of 5x11 dots, 8 character x 1 line display.

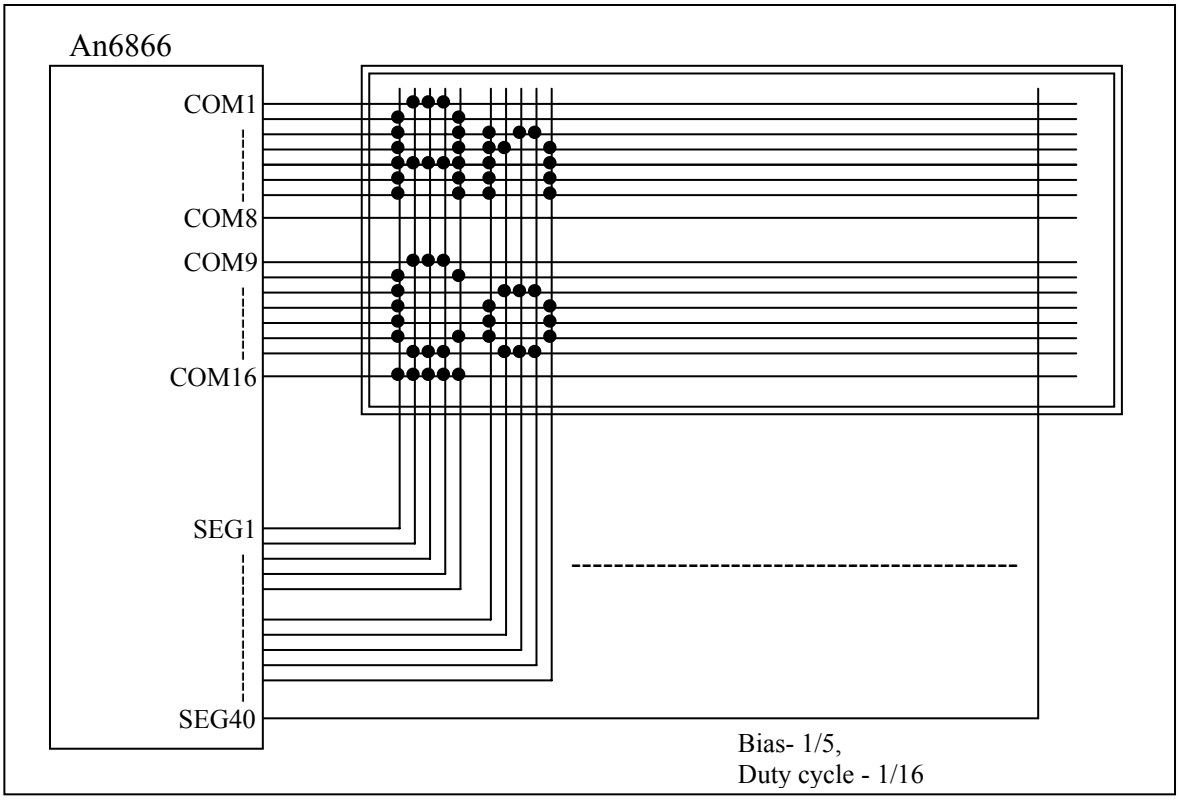


Figure 12. Example of 5x8 dots, 8 character x 2 line display (16 characters).

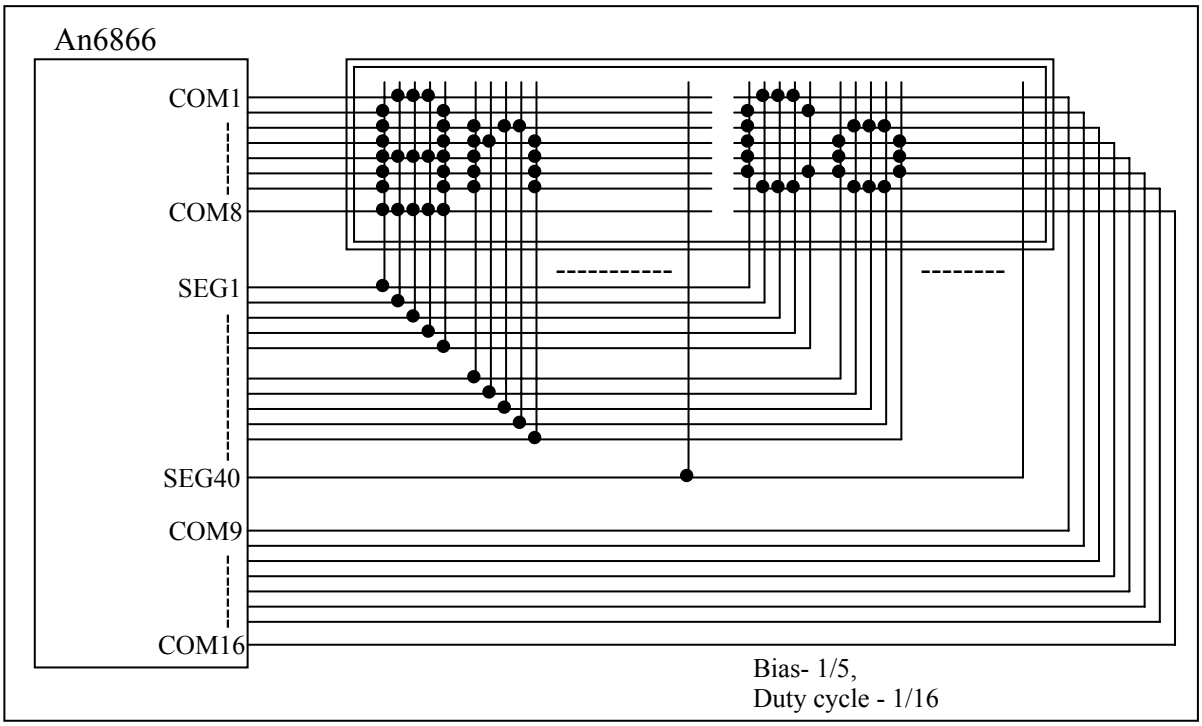


Figure 13. Example of 5x8 dots, 16 character x 1 line display (non-standard LCD layout).

4.3. Connection of the extension drivers

The An6866 can display up to 8 characters in one line with internal SEG drivers. To increase the number of displayed symbols, external drivers such as An6865 (40 SEG) or An6863 (80 SEG) are used. These chips contain their own SEG shift registers, which are cascade-connected to shift register output (D) increasing its length (see part 8.1).

Maximum register length and the corresponding number of displayed characters are limited by COM-line refresh cycle, and they are equal to 400 for 1-line mode (80 characters per line) and 200 for 2-line mode (40 characters per line).

Extension drivers are connected through 4-bit bus interface. This interface contains D shift register output, shift data strobe CLK2, latches strobe CLK1 and alternate LCD voltage signal M.

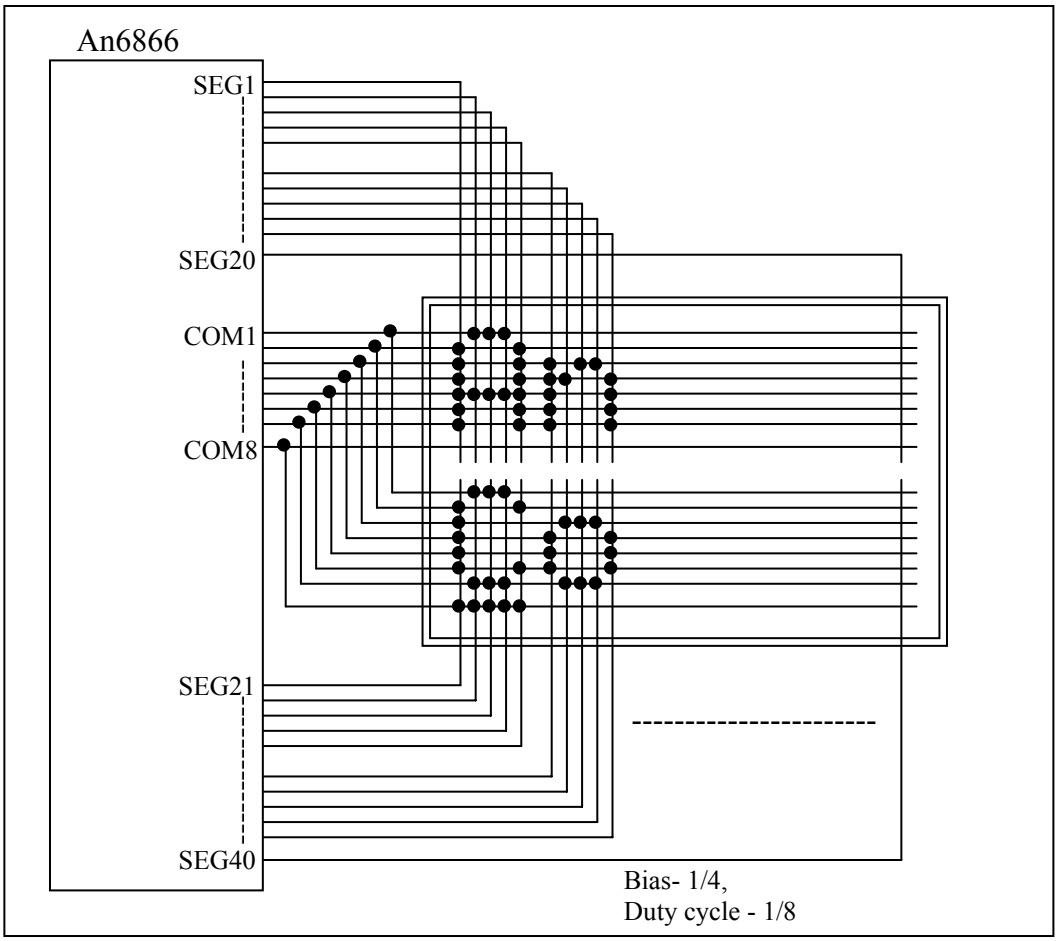


Figure 14. Example of 5x8 dots, 4 character x 2 line display (8 characters).

4.4. Power Supply for LCD Drive

COM and SEG drivers that output information directly to the LCD, form a complex multilevel timing diagram (see Figure 17-19).

Maximum voltage applied to LCD is V_{LCD}=VDD-V5. All this voltage range, with resistive divider, is split into 5 levels with 1/4 bias or into 6 levels with 1/5 bias (see Figure 12). These voltages are supplied to V1-V5 controller pins.

Each driver circuit commutates these voltages in the following way: less voltage outputs to non-lighted pixels, and entire V_{LCD} voltage outputs to lighted pixels. Because of LCD sluggishness, even a short action of high V_{LCD} voltage to activite display pixels is enough for high contrast of display image.

Table 13 Bias for LCD driving

Duty cycle	1/8, 1/11	1/16
Bias	1/4	1/5
Power supply pin	Voltage level	
V1	VDD-1/4 V_{LCD}	VDD-1/5 V_{LCD}
V2	VDD-1/2 V_{LCD}	VDD-2/5 V_{LCD}
V3	VDD-1/2 V_{LCD}	VDD-3/5 V_{LCD}
V4	VDD-3/4 V_{LCD}	VDD-4/5 V_{LCD}
V5	VDD-V_{LCD}	VDD-V_{LCD}

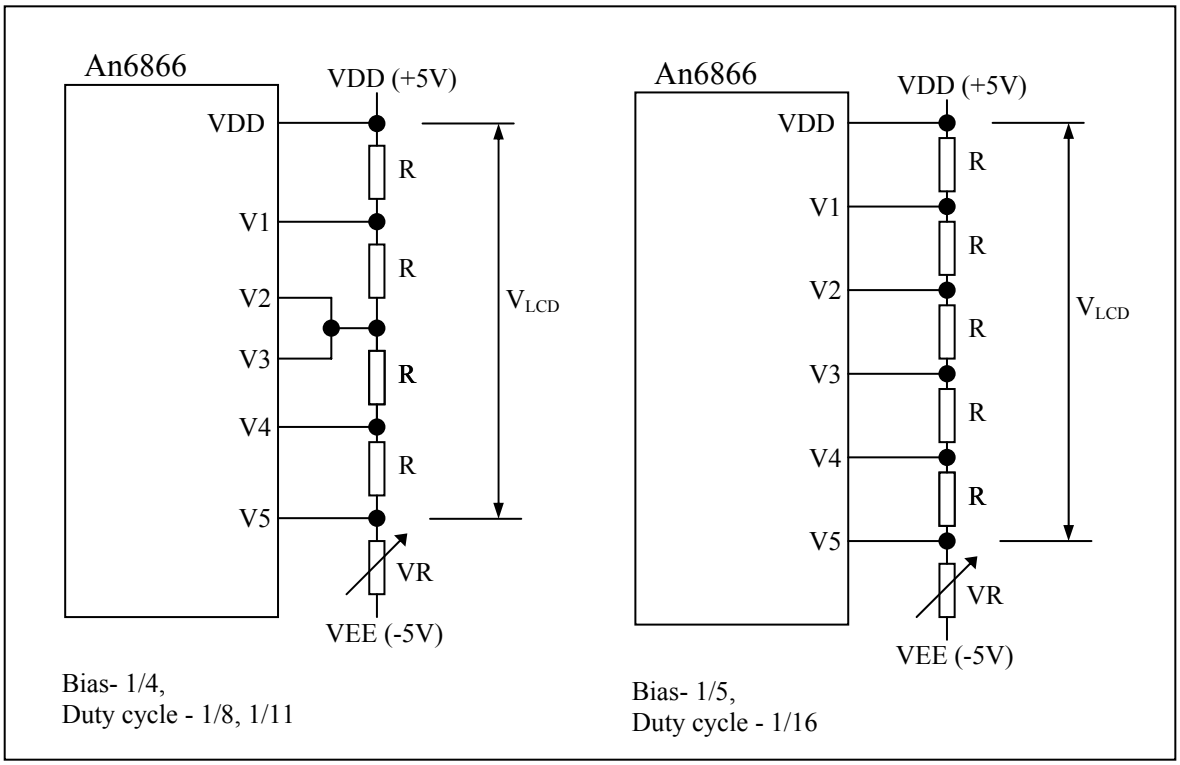


Figure 15. Drive Voltage Supply Example

On-chip V_{LCD} Bias Divider

The An6866 has on-chip V_{LCD} bias voltage divider resistors that can be connected internally to V1-V5 pads by a metal mask. The external resistors can be eliminated, but if required, they can be also connected for downward trimming of nominal divider resistances (Fig.16).

External voltage V_{LCD} is applied to contact pad V5. Voltages from pads V1-V4 can be applied to the An6865 or An6863 extension drivers (see the application circuit in Fig. 25). Nominal resistance values Rint for on-chip V_{LCD} bias divider resistors are selected within the following range:

- 4kΩ, 3kΩ, 2kΩ (4kΩ || 4kΩ), 1.7kΩ (4kΩ || 3kΩ), 1.5kΩ (3kΩ || 3kΩ).

The resistance tolerance is ±25%.

On-chip Clock Oscillator Resistor

The An6866 chip also contains an on-chip clock oscillator resistor (Fig.16). Its value is several times higher than that of an equivalent external resistor. The internal RC-circuits of the oscillator are adjusted so as to produce a predetermined nominal frequency value. The increased resistance makes it possible to further reduce the controller consumption current. When using an on-chip clock oscillator resistor two approaches to frequency tuning can be adopted:

- Nominal frequency is 270kHz±15% at V_{DD}=5V. In this case at the supply voltage V_{DD}=3V the oscillator frequency will be 50-60kHz lower than the nominal frequency.
- Nominal frequency is 250kHz±15% at V_{DD}=3V. In this case at the supply voltage V_{DD}=5V the oscillator frequency will be 70-80kHz higher than the nominal value.

Additional frequency tuning can be performed:

- to get lower frequency values by using an external capacitor coupled to the OSC1 pin.
- to get higher frequency values by using an external resistor connected between OSC1 and OSC2 pins. The nominal value for this resistor should be selected with account for extra OSC1 interconnection capacitance.

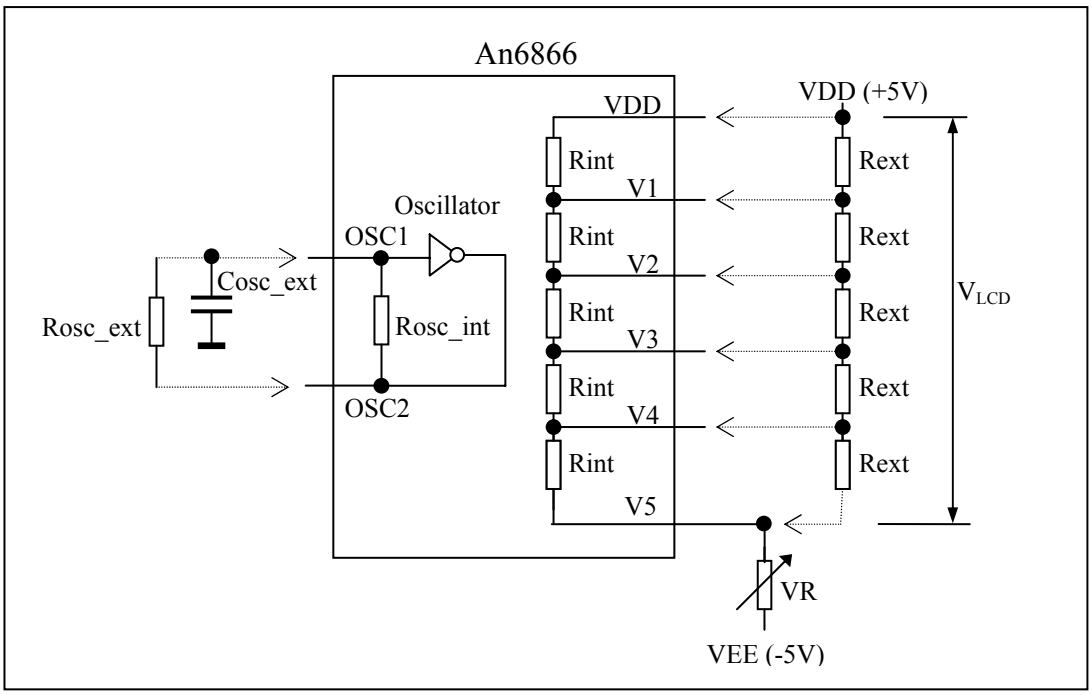


Figure 16. Connection of on-chip V_{LCD} bias divider resistors and on-chip clock oscillator resistor.

4.5. Display Waveform Timing Diagram

Image brightness depends on display waveform characteristics – the shorter is duty cycle, the higher is contrast. Duty cycle is determined by the number of active COM-lines. For 1-line mode duty cycle is 1/8 or 1/11, for 2-line mode duty cycle is 1/16.

Brightness is also determined by V_{LCD} and bias voltages V1-V5. Use of a divider with 1/5 bias ratio allows to obtain higher contrast than with 1/4 ratio.

To increase durability of the LCD, output drivers must alternate polarity of LCD supply voltage periodically. For this purpose the controller forms M signal. Two variants are possible:

- alternate V_{LCD} voltage polarity in each COM-line cycle. M state alternates two times in each COM cycle. M alternating frequency is equal to line frequency. This is "A" type of display waveform;
- alternate V_{LCD} voltage polarity in each frame cycle. M state alternates after full display update. M alternating frequency is equal to 1/2 of frame frequency. This is "B" type of display waveform.

The controller can work with both types of display waveforms. The type is determined by controller mask option (see part 3.5 and Appendix 1). Display waveform type is chosen separately for Standard and Extended modes, any combination is allowed.

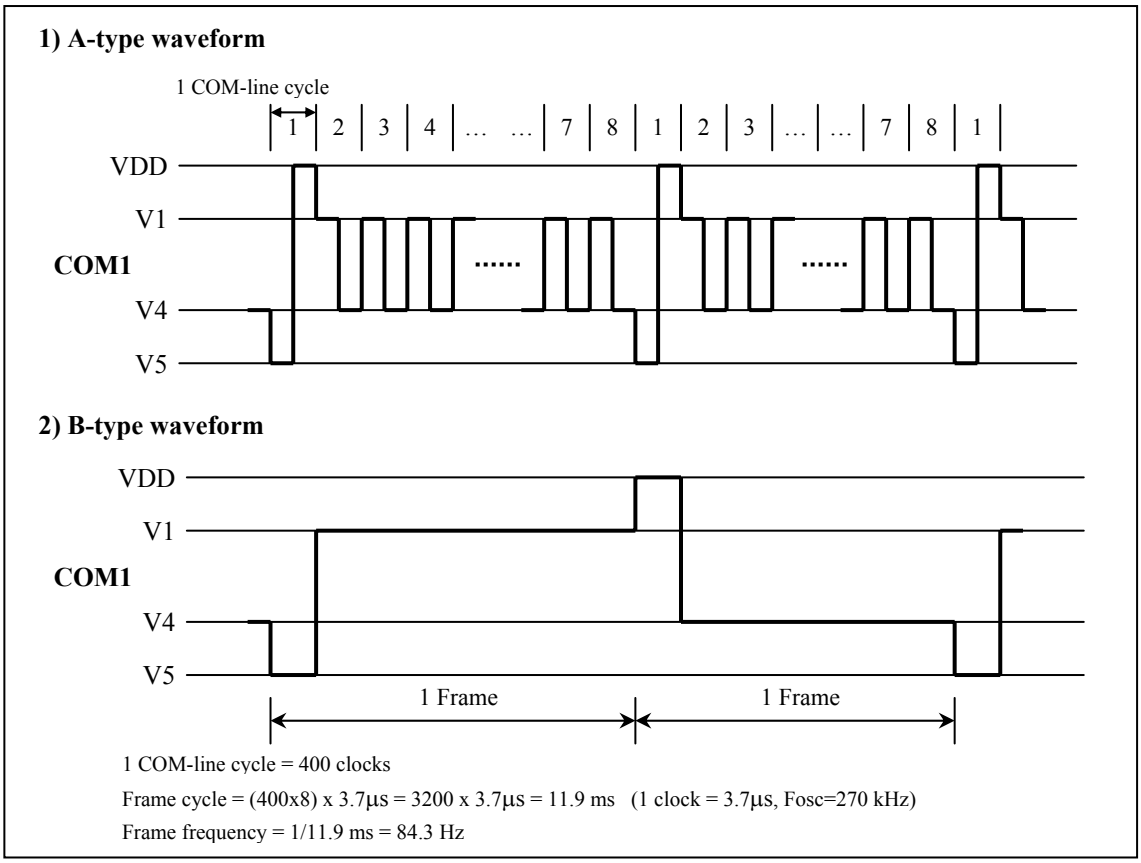


Figure 17. Timing diagram of Display Waveform for 1/8 duty cycle.

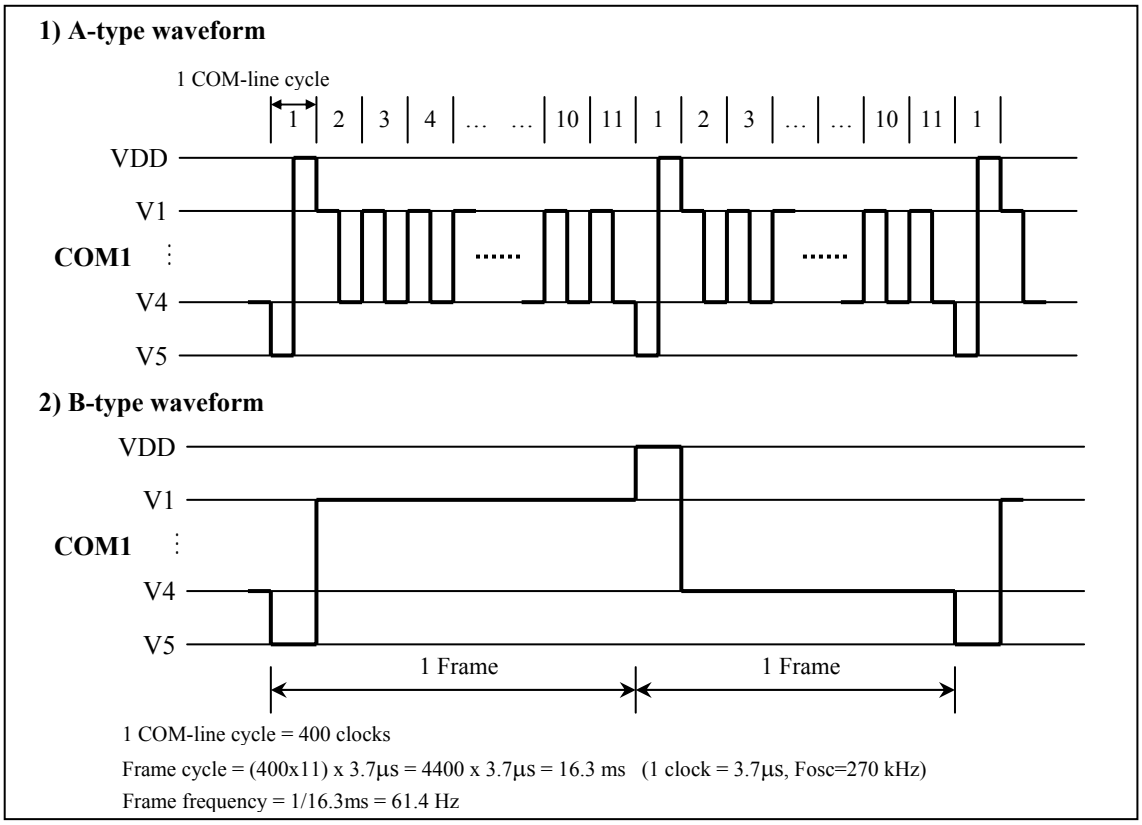


Figure 18. Timing diagram of Display Waveform for 1/11 duty cycle.

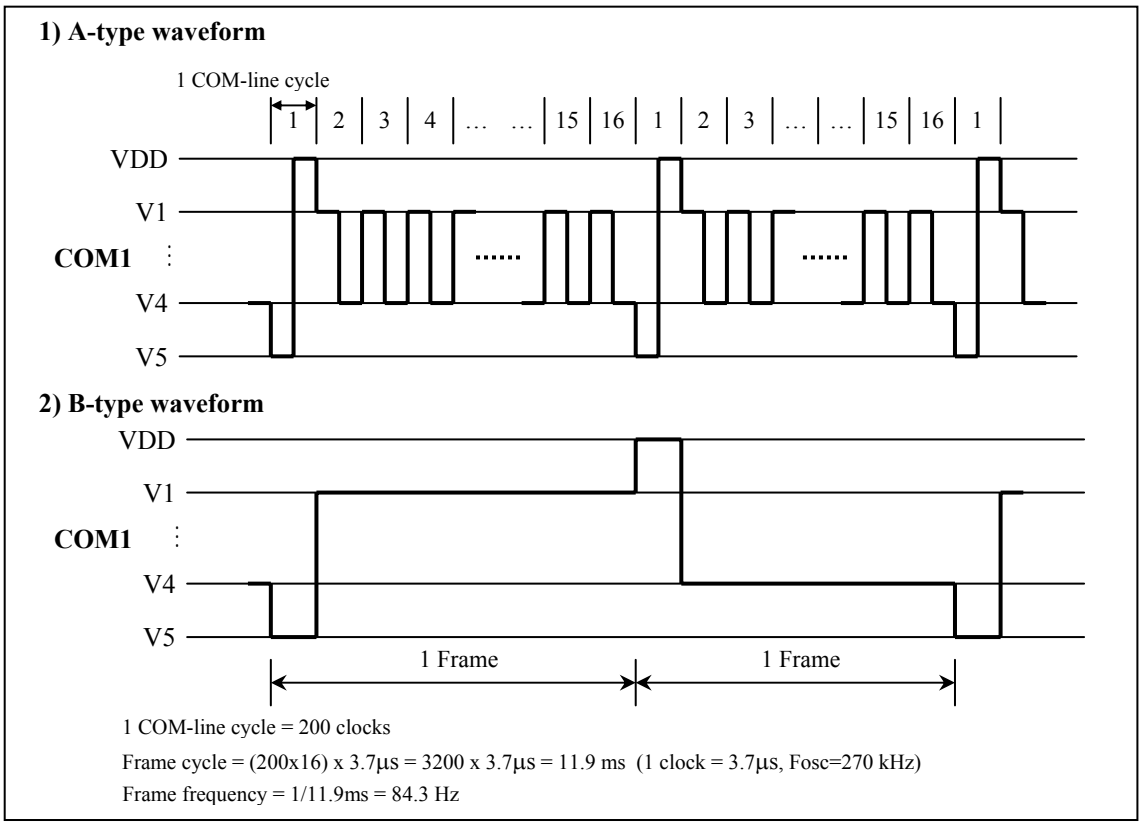


Figure 19. Timing diagram of Display Waveform for 1/16 duty cycle.

5. CONTROLLER PROGRAMMING

5.1. Initializing by instruction

Initializing by instruction in 8-bit interface mode

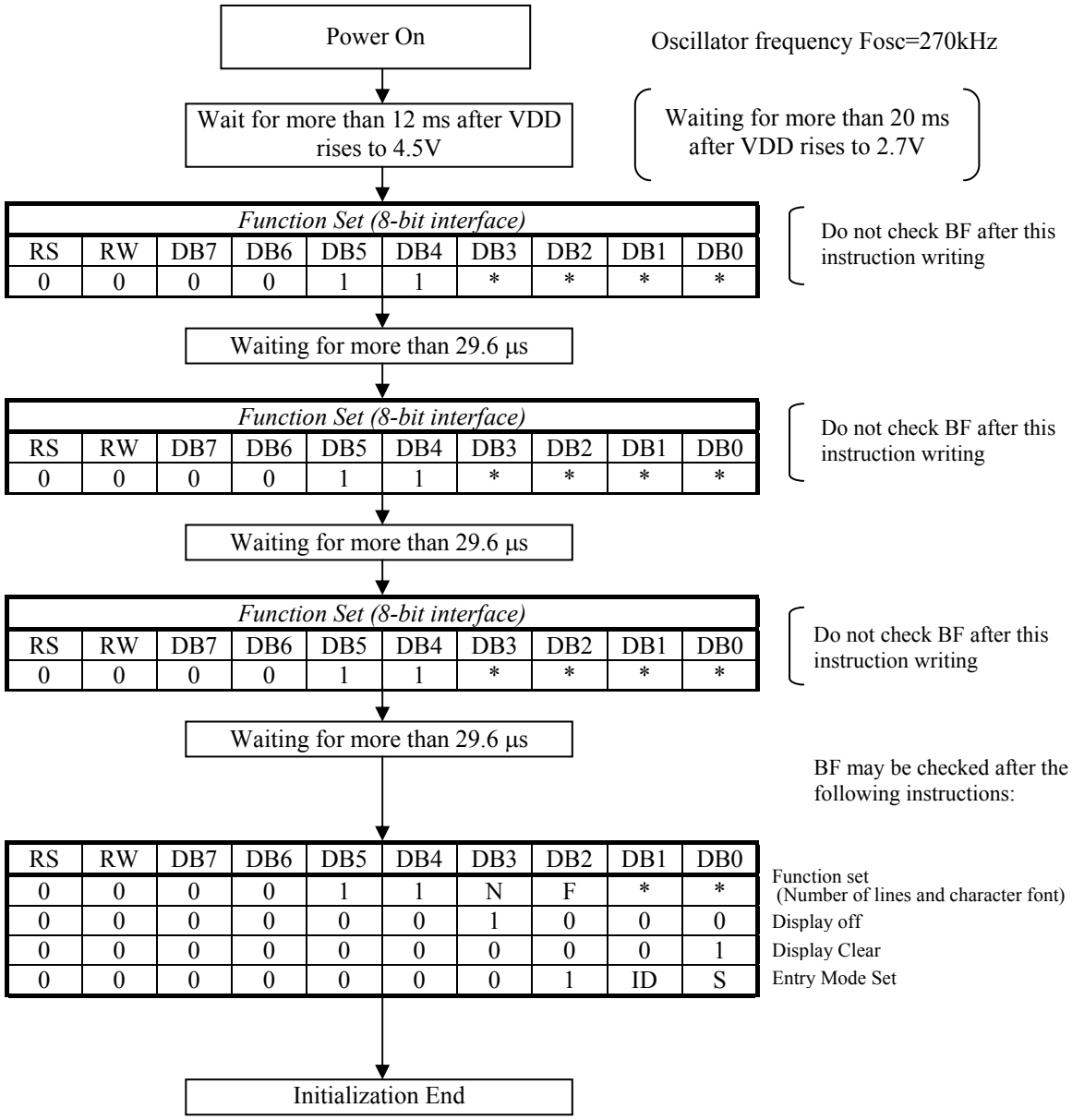


Figure 20. Initializing by instruction in 8-bit interface mode

Initializing by instruction in 4-bit interface mode

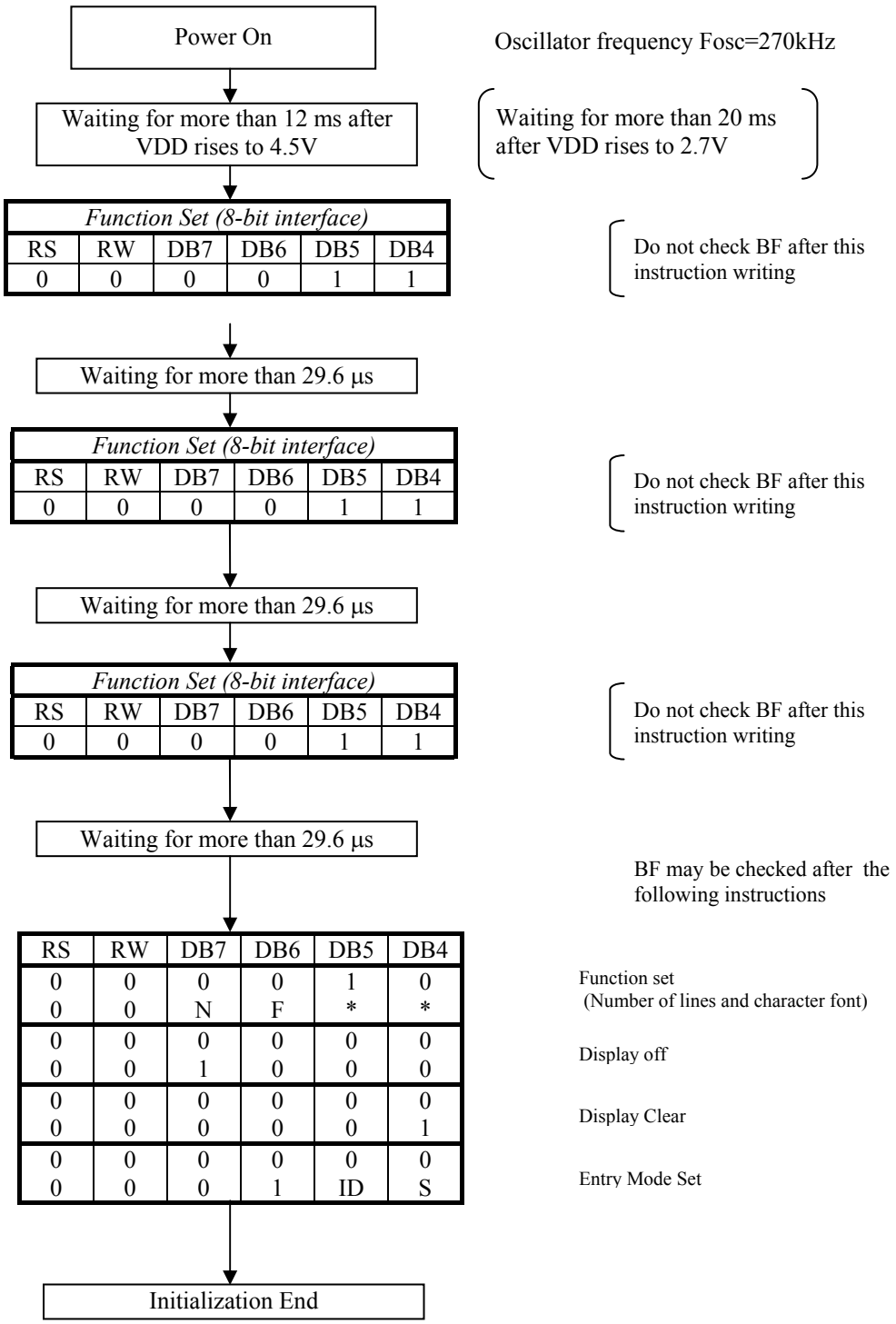


Figure 21. Initializing by instruction in 4-bit interface mode

5.2. Example of instruction and display correspondence in 8-bit interface mode

instruction sequence **LCD-panel**

1. Power Supply On: Initialized by the internal power on reset circuit

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

2. Function Set: 8-bit, 2 lines, 5x8 font

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	0	*	*

3. Display on, cursor on, blinking off

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	1	1	0

LCD-panel: _

4. Entry Mode Set: address increment

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	1	0

LCD-panel: _

5. Write Data to DDRAM: character A

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	0	0	0	1

LCD-panel: A_

6. Write Data to DDRAM: character N

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	1	1	1	0

LCD-panel: AN_

7. Write Data to DDRAM: character G

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	0	1	1	1

LCD-panel: ANG_

8. Write Data to DDRAM: character S

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	1	0	0	1	1

LCD-panel: ANGS_

9. Write Data to DDRAM: character T

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	1	0	1	0	0

LCD-panel: ANGST_

10. Write Data to DDRAM: character R

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	1	0	0	1	0

LCD-panel: ANGSTR_

11. Write Data to DDRAM: character E

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	0	1	0	1

LCD-panel: ANGSTRE_

12. Write Data to DDRAM: character M

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	1	1	0	1

LCD-panel: ANGSTREM

13. Set DDRAM Address: 40h

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	0	0	0	0	0	0

LCD-panel:
ANGSTREM
_

14. Write Data to DDRAM: character A

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	0	0	0	1

LCD-panel:
ANGSTREM
A_

15. Write Data to DDRAM: character n

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	1	0	1	1	1	0

```
ANGSTREM
An_
```

16. Write Data to DDRAM: character 6

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	0	1	1	0	1	1	0

```
ANGSTREM
An6_
```

17. Write Data to DDRAM: character 8

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	0	1	1	1	0	0	0

```
ANGSTREM
An68_
```

18. Write Data to DDRAM: character 7

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	0	1	1	0	1	1	1

```
ANGSTREM
An687_
```

19. Write Data to DDRAM: character 0

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	0	1	1	0	0	0	0

```
ANGSTREM
An6866_
```

20. Write Data to DDRAM: character space

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	0	1	0	0	0	0	0

```
ANGSTREM
An6866 _
```

21. Entry Mode Set: Display Shift on during write

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	1	1

```
ANGSTREM
An6866 _
```

22. Write Data to DDRAM: character L

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	1	1	0	0

```
NGSTREM
n6870 L_
```

23. Write Data to DDRAM: character C

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	0	0	1	1

```
GSTREM
6870 LC_
```

24. Write Data to DDRAM: character M

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	1	1	0	1

```
STREM
870 LCM_
```

25. Cursor or Display Shift: cursor moves left

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	0	0	1	0	0	*	*

```
STREM
870 LCM
```

26. Write Data to DDRAM: character D

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	0	1	0	0

```
TREM
70 LCD_
```

27. Return Home

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	0

```
ANGSTREM
An6866 L
```

28. Display Clear

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

```
_
```

5.3. Example of instruction and display correspondence in 4-bit interface mode

Instruction sequence **LCD-panel**

1. Power Supply On: Initialized by the internal power on reset circuit

RS	RW	DB7	DB6	DB5	DB4

2. Function Set: 4-bit, 2 lines, 5x8 font

RS	RW	DB7	DB6	DB5	DB4
0	0	0	0	1	0
0	0	0	0	0	0

3. Display on, cursor on, blinking off

RS	RW	DB7	DB6	DB5	DB4
0	0	0	0	0	0
0	0	1	1	1	0

4. Entry Mode Set: address increment

RS	RW	DB7	DB6	DB5	DB4
0	0	0	0	0	0
0	0	0	1	1	0

5. Write Data to DDRAM: character A

RS	RW	DB7	DB6	DB5	DB4
1	0	0	1	0	0
1	0	0	0	0	1

6. Write Data to DDRAM: character N

RS	RW	DB7	DB6	DB5	DB4
1	0	0	1	0	0
1	0	1	1	1	0

7. Write Data to DDRAM: character G

RS	RW	DB7	DB6	DB5	DB4
1	0	0	1	0	0
1	0	0	1	1	1

8. Write Data to DDRAM: character S

RS	RW	DB7	DB6	DB5	DB4
1	0	0	1	0	1
1	0	0	0	1	1

9. Write Data to DDRAM: character T

RS	RW	DB7	DB6	DB5	DB4
1	0	0	1	0	1
1	0	0	1	0	0

10. Write Data to DDRAM: character R

RS	RW	DB7	DB6	DB5	DB4
1	0	0	1	0	1
1	0	0	0	1	0

LCD-panel

_

_

A_

AN_

ANG_

ANGS_

ANGST_

ANGSTR_

Further instruction sequence is the same as in 8-bit interface mode (see part 5.2)

6. ELECTRICAL CHARACTERISTICS

6.1. Absolute Maximum Ratings

Parameter	Symbol	Unit	Value
Power supply voltage (1)	VDD	V	-0.3 to 7.0
Power supply voltage (2)	V_{LCD}	V	VDD-15 to VDD+0.3
Input voltage	V_{IN}	V	-0.3 to VDD+0.3

Note: VDD ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ V5.

6.2. Temperature Ratings

Parameter	Symbol	Unit	Value
Operating temperature	Topr	ºC	-30 to +85
Storage temperature	Tstg	ºC	-55 to +125

6.3. Power Supply Conditions Using Internal Reset Circuit

Parameter	Symbol	Conditions	Min	Typ	Max.	Unit
VDD rise time	t_{rVDD}	4.5V at VDD=4.5V÷5.5V 2.7V at VDD=2.7V÷4.5V	0.1	-	20	ms
VDD off time	t_{OFF}	0.2V	1	-	-	

6.4. Electrical characteristics for VDD = 4.5V ÷ 5.5V

(VDD=4.5V ÷ 5.5V, Ta= -30 ÷ +85ºC)

Parameter	Symbol	Conditions	Min	Typ	Max.	Unit
Operation Voltage	VDD	-	4.5	-	5.5	V
Supply Current	I_{DD}	RC-oscillator, external timing, VDD=5V, Fosc=270kHz, note 6.6.5	-	0.14	0.6	mA
Input Voltage (except OSC1)	V_{IH1}	-	2.2	-	VDD	V
	V_{IL1}	-	-0.3	-	0.6	
Input Voltage (OSC1)	V_{IH2}	-	VDD -1.0	-	VDD	
	V_{IL2}	-	-0.2	-	1.0	
Output Voltage (DB7-DB0)	V_{OH1}	I_{OH}= -0.205 mA	2.4	-	-	
	V_{OL1}	I_{OL}= 1.2 mA	-	-	0.4	
Output Voltage (except DB7-DB0)	V_{OH2}	I_{OH}= -40 µA	0.9 VDD	-	-	
	V_{OL2}	I_{OL}= 40 µA	-	-	0.1 VDD	
Voltage Drop on output drivers	Vd_{COM}	I_O= 0.1 mA, note 6.6.8	-	-	1	
	Vd_{SEG}		-	-	1	
Input Leakage Current	I_{IL}	V_{IN}= 0V ÷ VDD	-1	-	1	µA
Input Low Current RS, RW, DB0-DB7	I_{IN1}	V_{IN}= 0V, VDD=5V, (Pull-up to VDD), note 6.6.3	-40	-100	-180	
Input Low Current XMODE	I_{IN2}	V_{IN}= 0V, VDD=5V, (Pull-up to VDD), note 6.6.3	-6	-18	-50	
Internal Oscillator Frequency (with external resistor)	F_{IC}	Rf= 91KΩ ± 2%, VDD=5V, note 6.6.6	190	270	350	kHz
External Clock	F_{EC}	note 6.6.7	150	250	350	kHz
	duty		45	50	55	%
	rise time		-	-	0.2	µs
LCD Voltage	V_{LCD}	VDD-V5 (bias 1/5, 1/4)	4.6	-	13.0	V

Note: see part 6.6 "Electrical characteristics measurement conditions".

6.5. Electrical characteristics for VDD = 2.7V ÷ 4.5V

(VDD=2.7V ÷ 4.5V, Ta= -30 ÷ +85ºC)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operation Voltage	VDD	-	2.7	-	4.5	V
Supply Current	I_{DD}	RC-oscillator, external timing, VDD=3V, Fosc=270kHz, note 6.6.5	-	0.07	0.3	mA
Input Voltage (except OSC1)	V_{IH1}	-	0.7 VDD	-	VDD	V
	V_{IL1}	-	-0.3	-	0.4	
Input Voltage (OSC1)	V_{IH2}	-	0.7 VDD	-	VDD	
	V_{IL2}	-	-	-	0.2 VDD	
Output Voltage (DB7-DB0)	V_{OH1}	I_{OH}= -0.1 mA	2.0	-	-	
	V_{OL1}	I_{OL}= 0.1 mA	-	-	0.4	
Output Voltage (except DB7-DB0)	V_{OH2}	I_{OH}= -40 µA	0.8 VDD	-	-	
	V_{OL2}	I_{OL}= 40 µA	-	-	0.2 VDD	
Voltage Drop on output drivers	Vd_{COM}	I_O= 0.1 mA, note 6.6.8	-	-	1	
	Vd_{SEG}		-	-	1.5	
Input Leakage Current	I_{IL}	V_{IN}= 0V ÷ VDD	-1	-	1	µA
Input Low Current RS, RW, DB0-DB7	I_{IN1}	V_{IN}= 0V ÷ VDD, (Pull-up to VDD), note 6.6.3	-10	-40	-90	
Input Low Current XMODE	I_{IN2}	V_{IN}= 0V, VDD=3V, (Pull-up to VDD), note 6.6.3	-1.5	-6	-15	
Internal Oscillator Frequency (with external resistor)	F_{IC}	Rf= 75 KΩ ± 2%, VDD=3V, note 6.6.6	190	270	350	kHz
External Clock	F_{EC}	note 6.6.7	150	250	350	kHz
	duty		45	50	55	%
	rise time		-	-	0.2	µs
LCD Voltage	V_{LCD}	VDD-V5 (bias 1/5, 1/4)	3.0	-	13.0	V

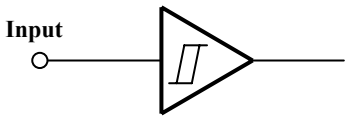
Note: see part 6.6 "Electrical characteristics measurement conditions".

6.6. Electrical characteristics measurement conditions

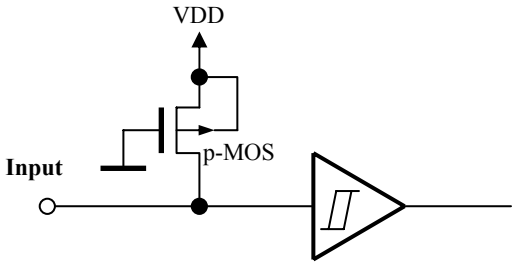
1) VDD≥V1≥V2≥V3≥V4≥V5.

2) Controller input/output pins circuit diagrams (except LCD output drivers):

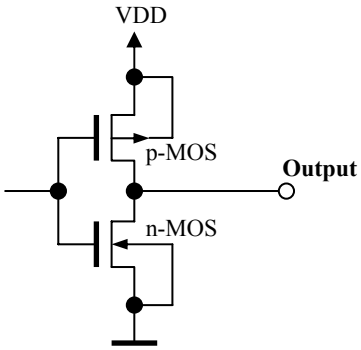
E pin (CMOS input without pull-up)



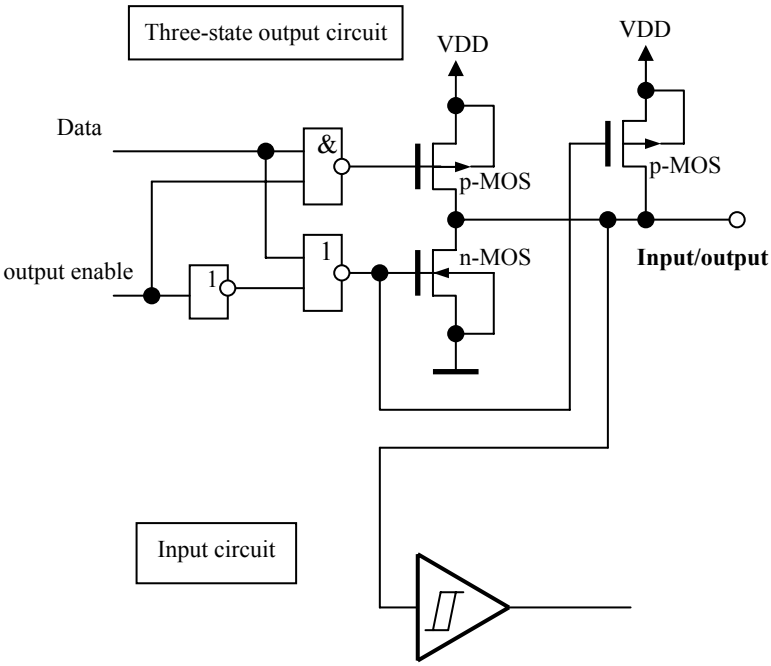
RS, RW pins (CMOS with pull-up)



CLK1, CLK2, D, M pins (CMOS output)



DB0-DB7 pins (CMOS input/output with pull-up)

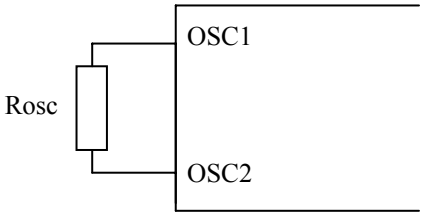


3) Pull-up current for input/output pins is measured only through pull-up transistor. Input/output current is excluded.

4) MPU interface input buffers use Schmitt trigger circuit with hysteretic not less than 0.15V (at VDD=5V).

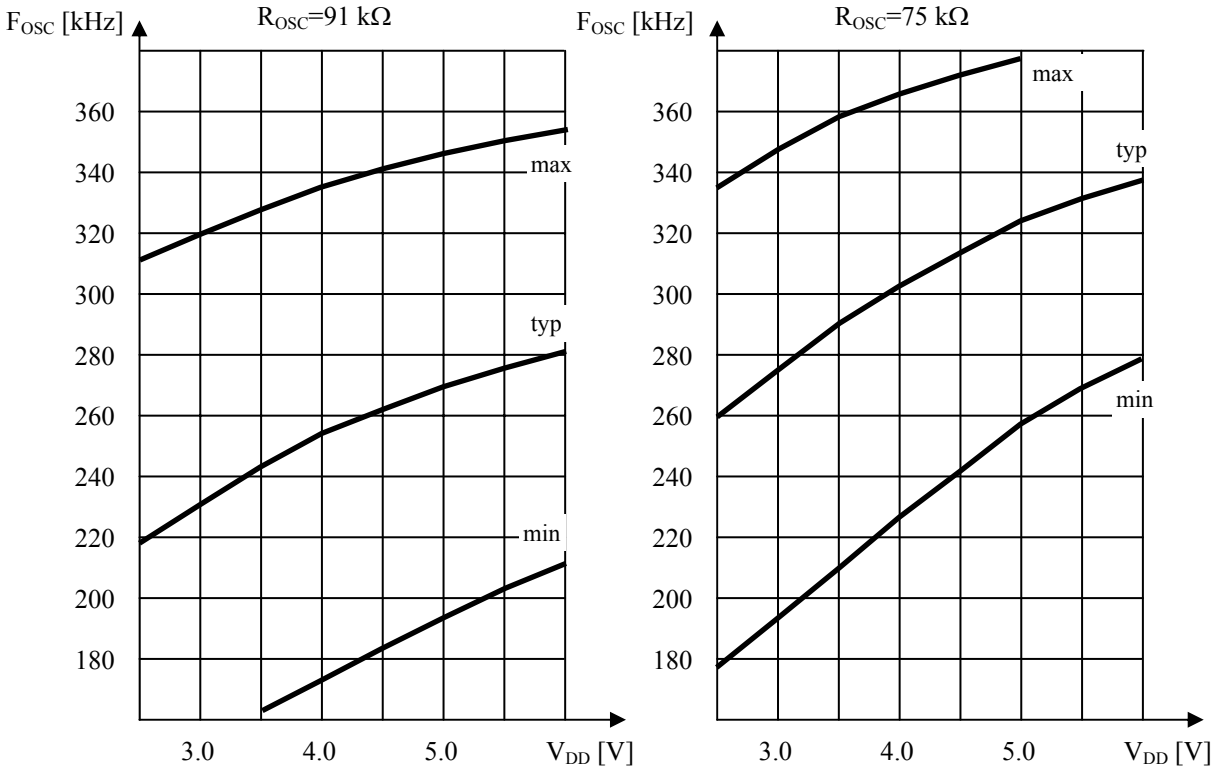
5) Consumption current does not include input/output currents. Consumption current is measured under the following conditions:
   - If intermediate levels are set for controller inputs, additional current from power supply flows through input buffer. To exclude this situation, input pins level must be fixed to GND or VDD;
   - Inputs and outputs with pull-up to VDD must have VDD level or be disconnected;
   - Resistive or capacitive output loads are absent.

6) External oscillator resistor connection:

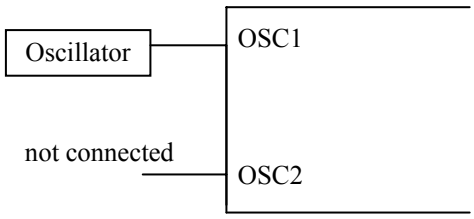


Rosc = 75 kΩ ±2% (at VDD=3V)
Rosc = 91 kΩ ±2% (at VDD=5V)

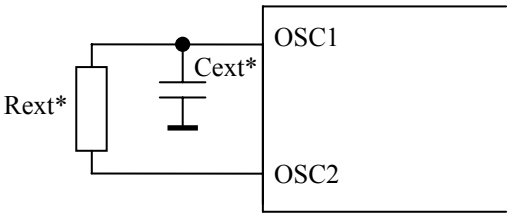
External capacitance at OSC1 influences the oscillator frequency. To decrease this influence, the length of pin wires for OCS1 and OSC2 must be minimal.



7) External oscillator connection:



8) Using an on-chip clock oscillator resistor:



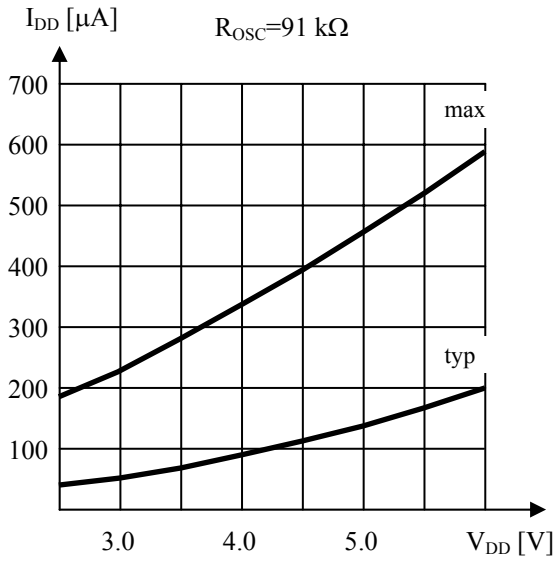
Elements designated by * are used for clock frequency tuning:

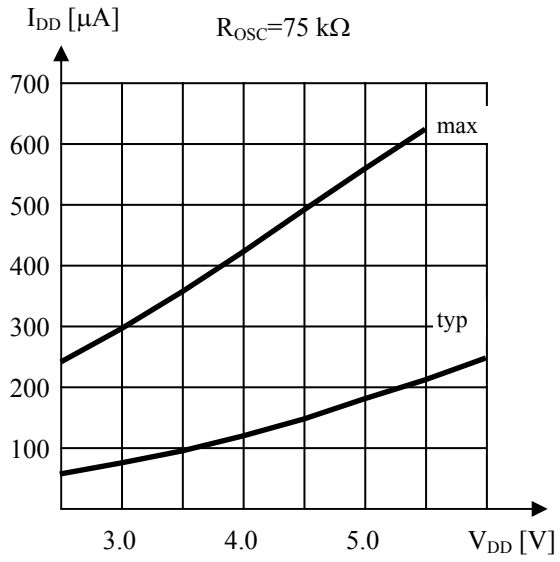
Rext* valued 500kΩ to 1500kΩ (depending on the external OSC1 circuit capacitance) is used to increase clock frequency.

Cext* valued 1.5pF to 2.5pF is used to decrease clock frequency.

9) COM and SEG outputs without load provide ±0.15V precision of output voltage relatively to V_{LCD} (VDD, V1, V2, V3, V4, V5).

10) The next diagrams show the consumption current vs. VDD dependence at R_{OSC} fixed. (Oscillator frequency variates according the VDD change - see part 6).





7. AC CHARACTERISTICS

7.1. VDD = 4.5V ÷ 5.5V

(VDD=4.5V ÷ 5.5V, Ta= -30 ÷ +85ºC)

Mode	Parameter	Symbol	Min	Max	Unit
Write Mode (Figure 22)	E Cycle Time	t_C	500		ns
	E Rise / Fall Time	t_r, t_f		20	
	E Pulse Width (High, Low)	t_W	230		
	RW and RS Setup Time	t_{SU1}	40		
	RW and RS Hold Time	t_{H1}	10		
	Data Setup Time	t_{SU2}	80		
	Data Hold Time	t_{H2}	10		
Read Mode (Figure 23)	E Cycle Time	t_C	500		ns
	E Rise / Fall Time	t_r, t_f		20	
	E Pulse Width (High, Low)	t_W	230		
	RW and RS Setup Time	t_{SU}	40		
	RW and RS Hold Time	t_H	10		
	Data Output Delay Time	t_D		120	
	Data Hold Time	t_{DH}	5		

7.2. VDD = 2.7V ÷ 4.5V

(VDD=2.7V ÷ 4.5V, Ta= -30 ÷ +85ºC)

Mode	Parameter	Symbol	Min	Max	Unit
Write Mode (Figure 22)	E Cycle Time	t_C	1000		ns
	E Rise / Fall Time	t_r, t_f		25	
	E Pulse Width (High, Low)	t_W	400		
	RW and RS Setup Time	t_{SU1}	60		
	RW and RS Hold Time	t_{H1}	20		
	Data Setup Time	t_{SU2}	195		
	Data Hold Time	t_{H2}	10		
Write Mode (Figure 23)	E Cycle Time	t_C	1000		ns
	E Rise / Fall Time	t_r, t_f		25	
	E Pulse Width (High, Low)	t_W	450		
	RW and RS Setup Time	t_{SU}	60		
	RW and RS Hold Time	t_H	20		
	Data Outpu Delay Time	t_D		360	
	Data Hold Time	t_{DH}	5		

7.3. Driver Interface Characteristics

Mode	Parameter	Symbol	Min	Max	Unit
Interface Mode with Extension Driver (Figure 24)	CLK1, CLK2 High Pulse Width	t_{WH}	800		ns
	CLK2 Low Pulse Width	t_{WL}	800		
	Clock Rise/Fall Time	t_r, t_f		25	
	CLK2 Setup Time	t_{SU1}	500		
	Data Setup Time	t_{SU2}	300		
	Data Hold Time	t_{DH}	300		
	M Delay Time	t_{DM}	-1000	1000	

7.4. Controller Interfaces Timing Diagrams

Write operation

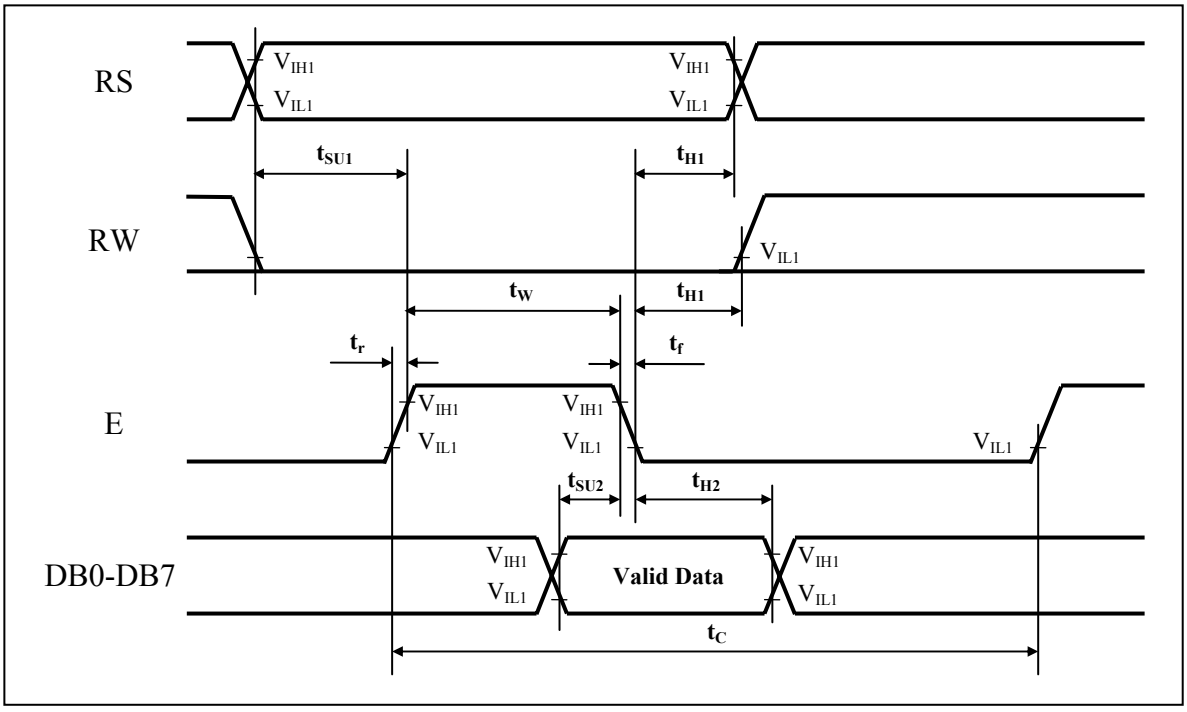


Figure 22. Write Mode Timing Diagram

Read operation

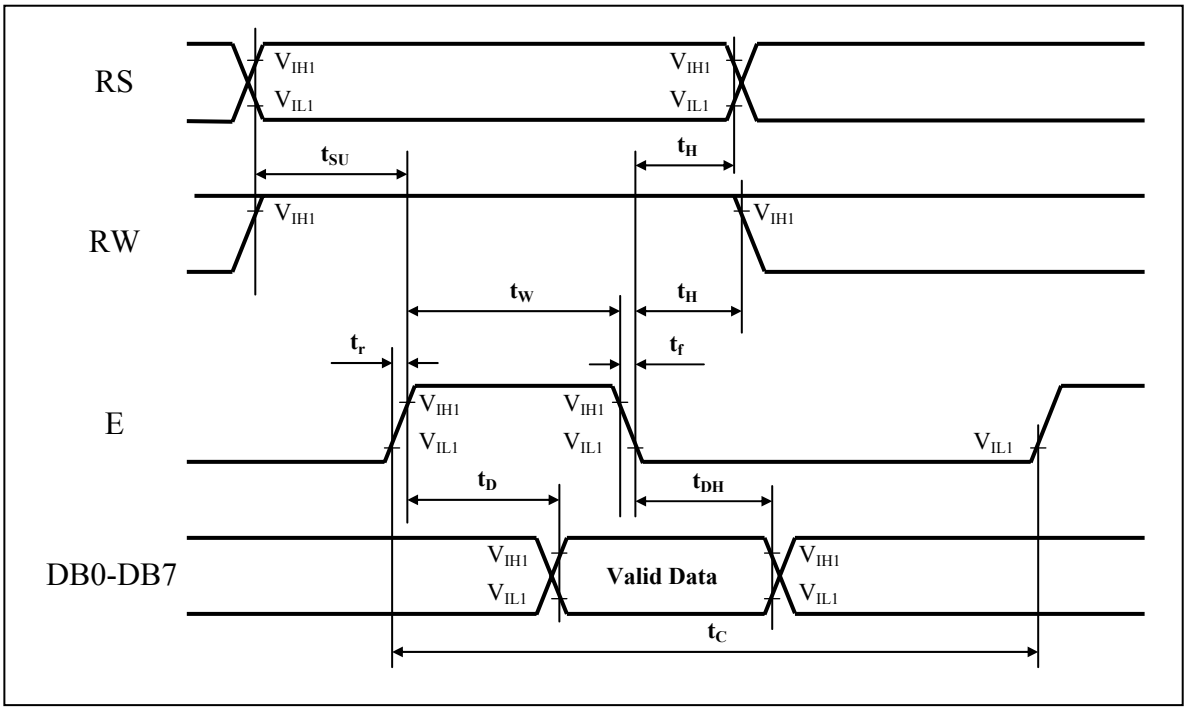


Figure 23. Read Mode Timing Diagram

Extension driver interface

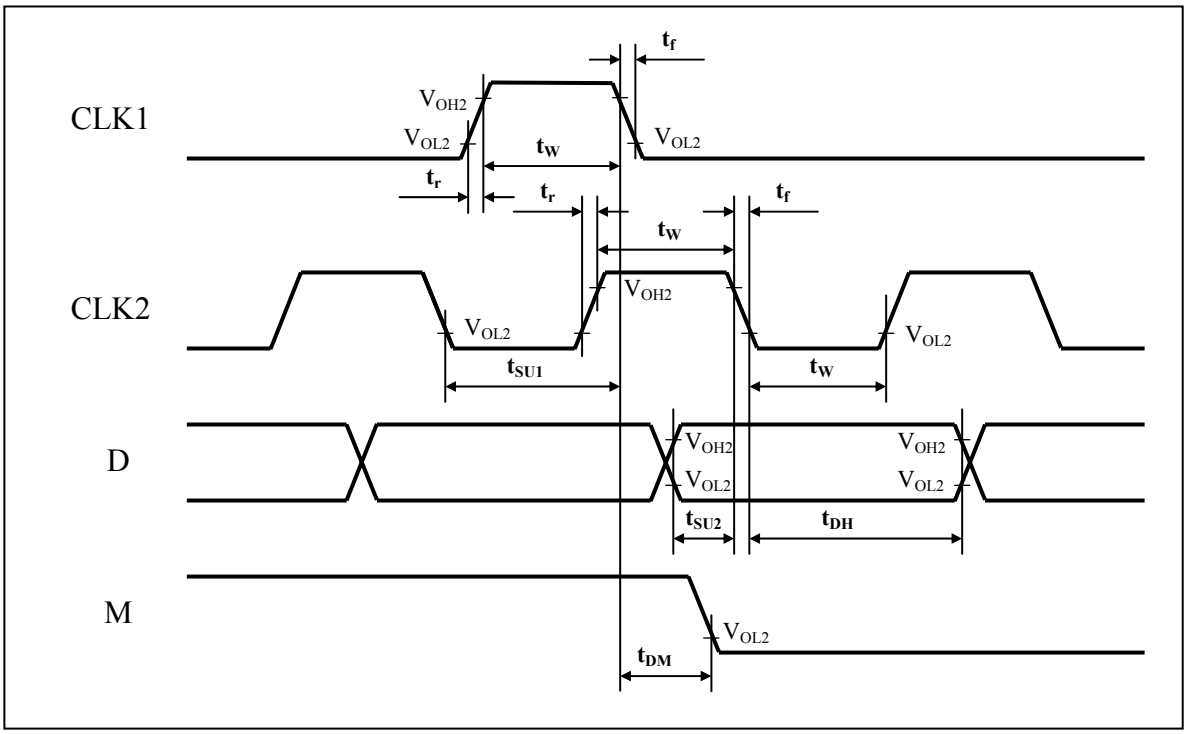


Figure 24. Extension Driver Interface Timing Diagram

8. APPLICATION INFORMATION

8.1. Application example of An6866 with extension drivers.

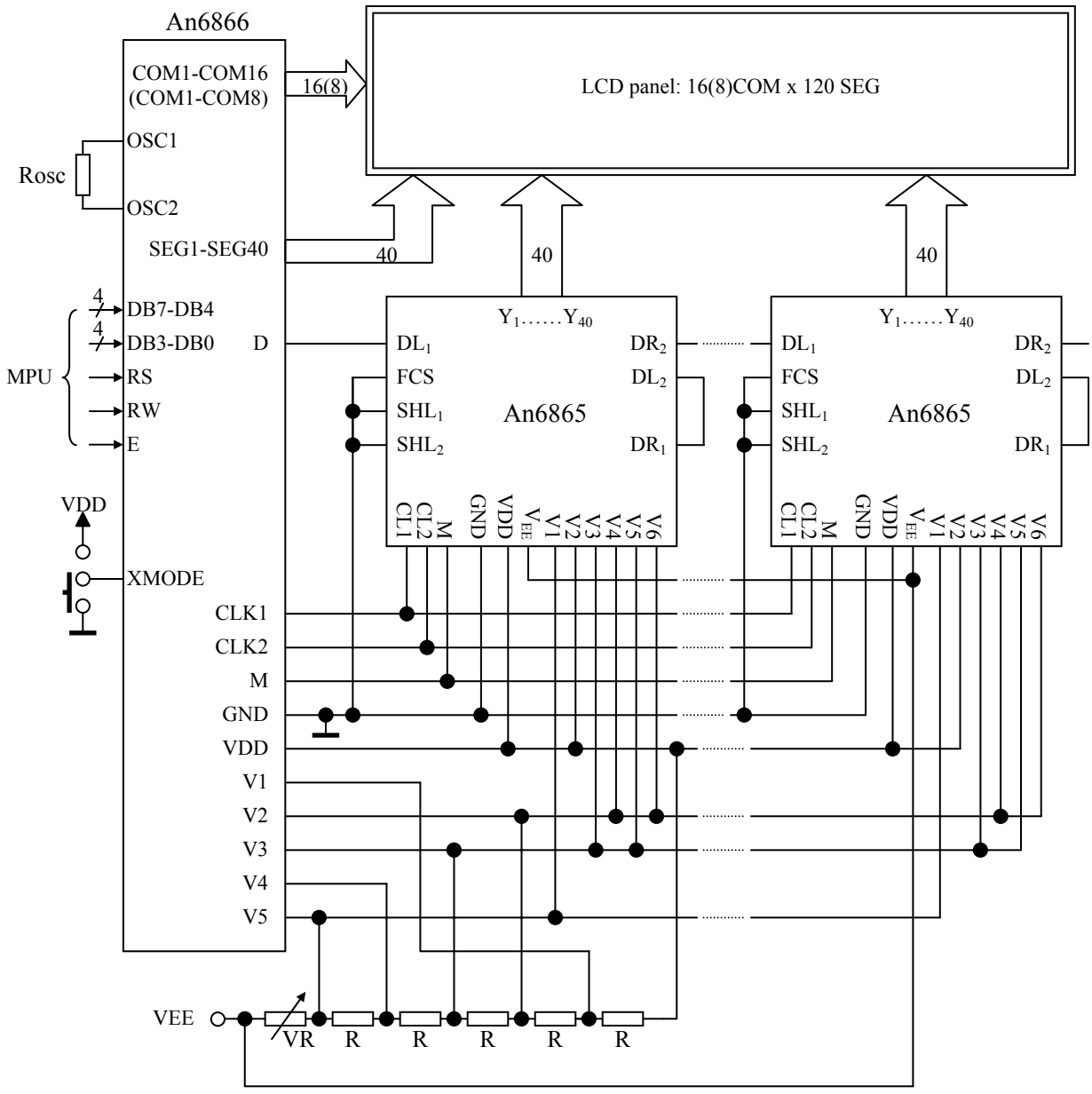


Figure 25. Application circuit of An6866.

8.2. Fast instruction executing mode

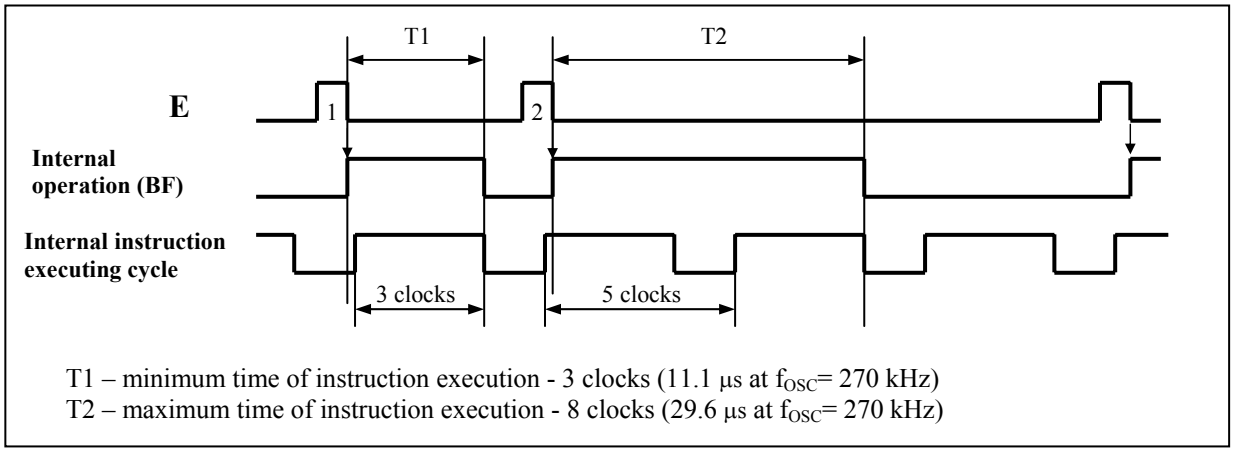
During the sequential execution of continuous instructions chain, there may be a situation, when every instruction will be executed in 5 clocks.

Figure 26 clarifies the conditions about different times of instruction executing. Instructions are executed during the appropriate phase 3 clocks long and 5 clocks period (see also part 2.6 "Timing Diagram"). Each instruction must pass one complete interval of the executing phase. Instruction executing begins at E fall and finishes at the end of the complete executing phase; BF has the same high level duration.

Figure 26 shows that instruction 1 is executed for approximately 3 clocks, because it is written directly before the executing phase. Instruction 2 comes after the beginning of the current executing phase, that is why it is executed for 5 clocks longer (approximately 8 clocks).

If MPU is capable to define the low level of BF and to write the next instruction during 2 clocks (7.4μs at f_{OSC}= 270kHz), which passes from the moment of completing of the previous phase of instruction executing till the beginning of the next one, then the instructions will be executed in every executing phase, i.e. at the highest speed when the sequential instruction writing. At that, writing and executing cycle for each instruction, beginning from the second one, will contain exactly 5 clocks (18.5μs at f_{OSC}= 270kHz).

Figure 27 shows one of the possible ways for fast instruction executing.



T1 – minimum time of instruction execution - 3 clocks (11.1 μs at f_{OSC}= 270 kHz)
T2 – maximum time of instruction execution - 8 clocks (29.6 μs at f_{OSC}= 270 kHz)

Figure 26. Instruction execution time

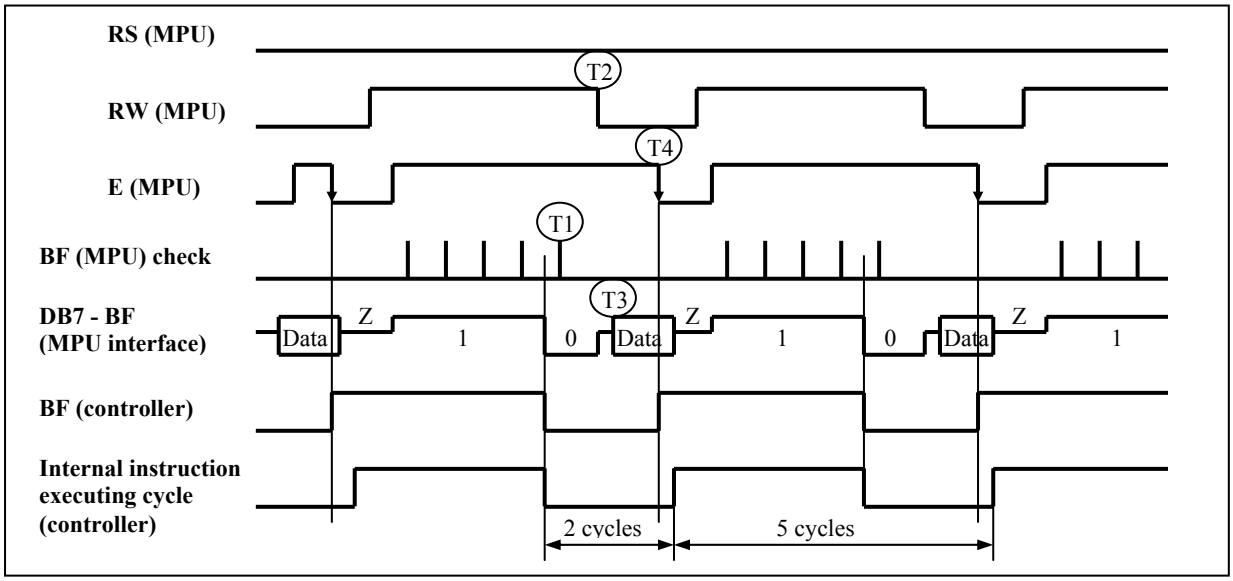


Figure 27. Example of fast instruction execution

After writing the instruction MPU releases DB bus, then sets Read BF and Address mode and high E level. Polling DB7 output, MPU waits till BF state becomes 0 (T1).

After that MPU switches to instruction write mode (T2), then it sets new data (T3) and writes the next instruction at E fall (T4). If MPU executes these operations during less than 2 clocks, then the new instruction will begin executing already in the next instruction executing phase, at that, duration of write and execute instruction period will be 5 clocks.

8.3. Sleep mode

The An6866 allows to use the sleep mode because the internal controller circuit has no floating nodes. All tri-states nodes have active pull-up to VDD in Z-state.

In the sleep mode the controller does not generate display waveform and does not accept instructions, but it keeps its state and memory content. Operation current in the sleep mode (I_{DD}) is significantly reduced (typical value is less then 15 μA).

To switch the controller to the sleep mode it is necessary to stop the oscillator and disconnect bias divider resistors from power supply. Before switching to the sleep mode, it is recommended to execute the Display Off instruction (see part 2.10), so that the controller would not switch to the sleep mode during the memory access operation.

Switching to the sleep mode is made by hardware (see Figure 28). It is better to stop the oscillator at the OSC2 pin not to add parasitic capacity in OSC1 pin. It is not recommended to leave OSC1 pin open, because it has no active pull-up.

The simplest way to stop oscillator is connecting OCS1 pin to GND or VDD. But in this case additional current from power supply will flow through R_{OSC} (~55 μA at VDD=5V and R_{OSC}=91 kΩ).

Bias divider resistors can be commutated both at VDD and VEE circuit.

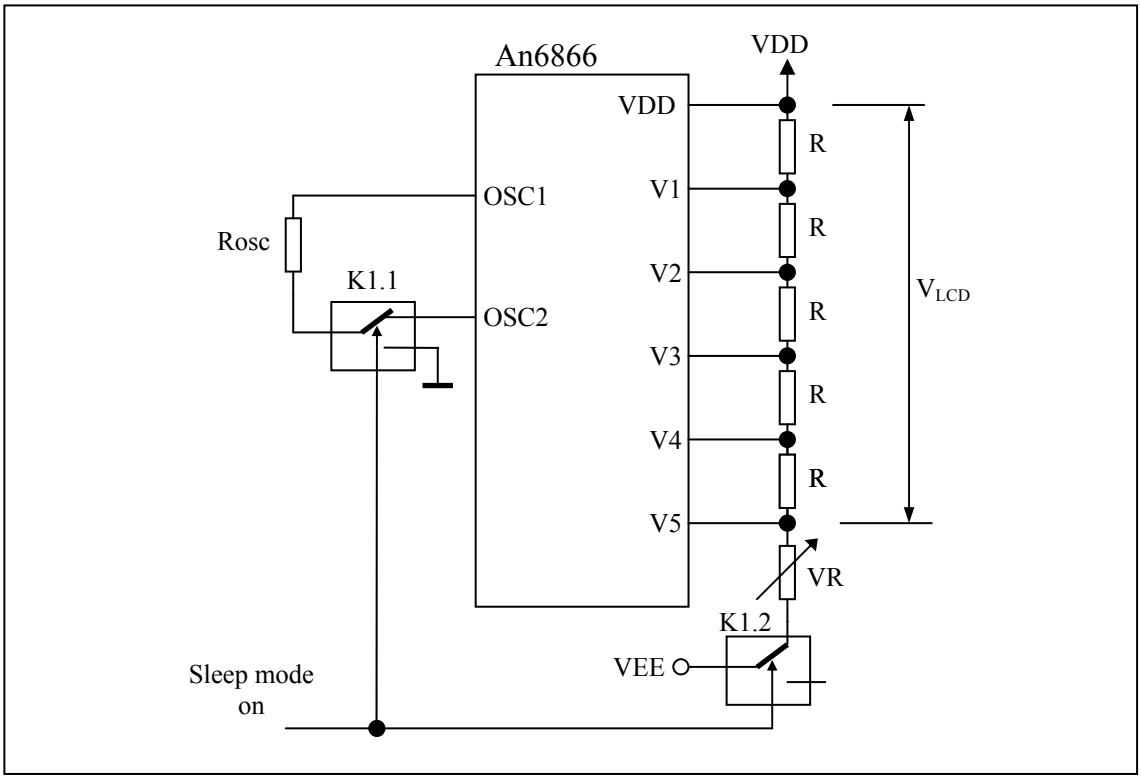


Figure 28. Sleep mode

8.4. Software estimation of oscillator frequency

Software estimation of oscillator frequency is based on evaluation of time interval between two events, depending from oscillator frequency.

It is possible to use BF and address reading procedure and any instruction that changes AC value.

Frequency determination is made the following way (see Figure 29):

MPU should write instruction that changes AC value (for example, Cursor Move). Then the controller is quickly switched into BF and address reading mode. It has minimum 1.5 cycles for this operation. Time interval T between moment of AC change and moment of BF resetting to 0 is exactly 1.5 clocks of oscillator timing diagram.

Oscillator frequency $\mathbf{F_{OSC} = 1.5/T.}$

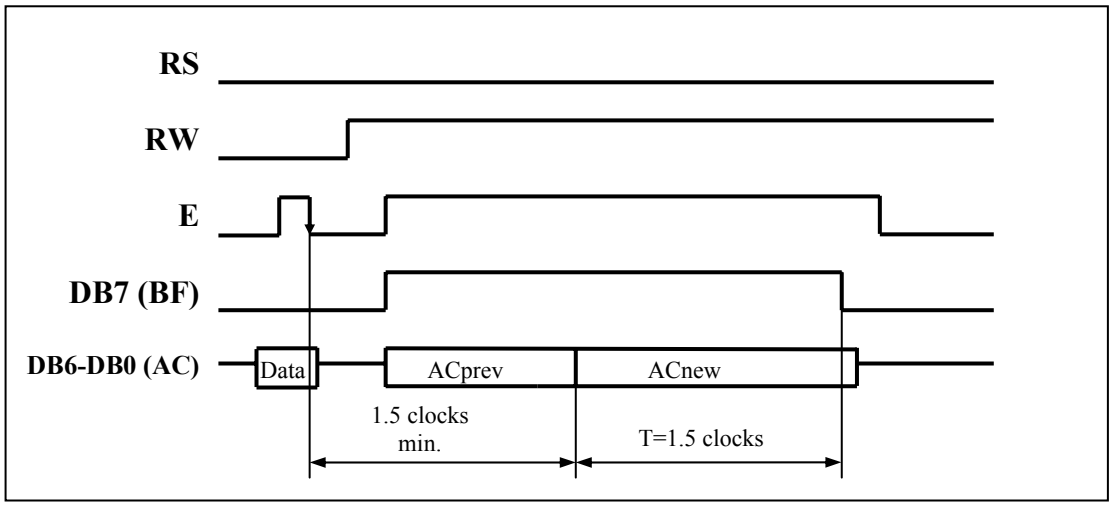


Figure 29. Software determination of oscillator frequency.

8.5. Working with 7-segment display.

The AN6866 can drive the 7-segment display. Combination of dot matrix display with 7-segment display is also possible.

CGRAM with information for segment lighting is used to control 7-segment display.

Example of system with dot matrix 8-character display and 4-line 7-segment display is shown in figure 30.

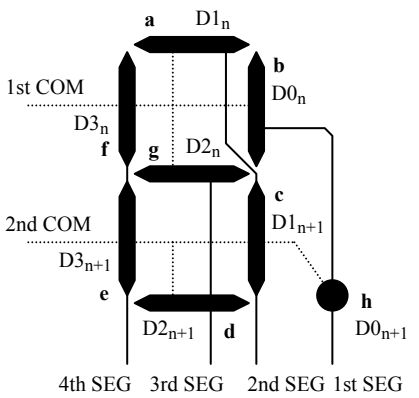
For displaying complex information 2-line mode is used. COM1-COM8 (first character line) are used to output four 8-digit numbers (totally 32 7-segment digits with decimal points). COM9-COM16 (second character line) are used to display 8 dot matrix characters.

Before using this mode, the controller must be initialized. The following settings must be executed:

1. to set 2-line mode by Function Set instruction with N=1;
2. to perform CGRAM initialization: to execute Set CGRAM Address instruction and to write 64 zero bytes or information for displaying (see below);
3. to execute Set DDRAM Address instruction with AC=0 and to write CGRAM codes from 0 to 7 into the first 8 DDRAM bytes.

Each 7-segment digit occupies 2 COM-lines and 4 SEG-rows. 2 contiguous bytes with 4 significant bits D3-D0 in each byte are used to operate segments of one digit. Correspondence between CGRAM data bits and lighting segments of the one 7-segment digit is shown in Table 14.

Table 14. Correspondence between CGRAM bits and lighting segments



Segment	COM	SEG	CGRAM
a	1	2	$D1_n$
b	1	1	$D0_n$
c	2	2	$D1_{n+1}$
d	2	3	$D2_{n+1}$
e	2	4	$D3_{n+1}$
f	1	4	$D3_n$
g	1	3	$D2_n$
h	2	1	$D0_{n+1}$

Note. Relative numeration SEGs and COMs for one 7-segment digit is shown. "n" and "n+1" – current and next CGRAM bytes position; D3-D0 – bits of corresponding CGRAM byte.

For the 1st character control CGRAM bytes 00h and 01h are used, for the second character – bytes 02h-03h etc. Totally 32 7-segment characters can be controlled by 64 CGRAM bytes.

To jump to the next digit, AC must be incremented by 8. At sequential AC incrementing, digits on display will be counted in vertical direction (see figure 28).

It is possible to use 5th SEG of each character. With this SEG output, various delimiters and other elements (icons) may be lighted. This SEG output is controlled by D4 bit of proper CGRAM byte.

Note, that it is difficult to use the cursor and blinking for 7-segment digits in practice. The cursor is displayed in COM8 line and lights the lower part of the 4th line of 7-segment digit. However, if the 4th 7-segment line is excluded, then COM8 may be used for displaying cursor for one 7-segnment digit line (totally 8 positions). Blinking influences all the four digits in vertical column, because all of them are controlled by the same SEGs.

Display Shift instruction for 7-segment display part works correctly, but for additional elements (icons, etc) it does not, if they are not in regular order.

Display Clear instructions works correctly, but repeated initialization of DDRAM area for 7-segment characters is needed (see point 3 above). CGRAM contents is kept, therefore, information on display is restored after DDRAM initialization.

If placement of dot characters line and 7-segment lines is interchanged, then dot matrix character line starts at 0 byte of DDRAM, and array of 7-segment digits – at 40 byte of DDRAM. Changes in initialization procedure must also be executed. Display Clear and Return Home instructions move the cursor to the beginning of dot matrix characters line.

For better results in displaying 7-segment digits, it is recommended to use controller version with B-type display waveform, because it is more convenient to use with various output capacitance loads on LCD drivers.

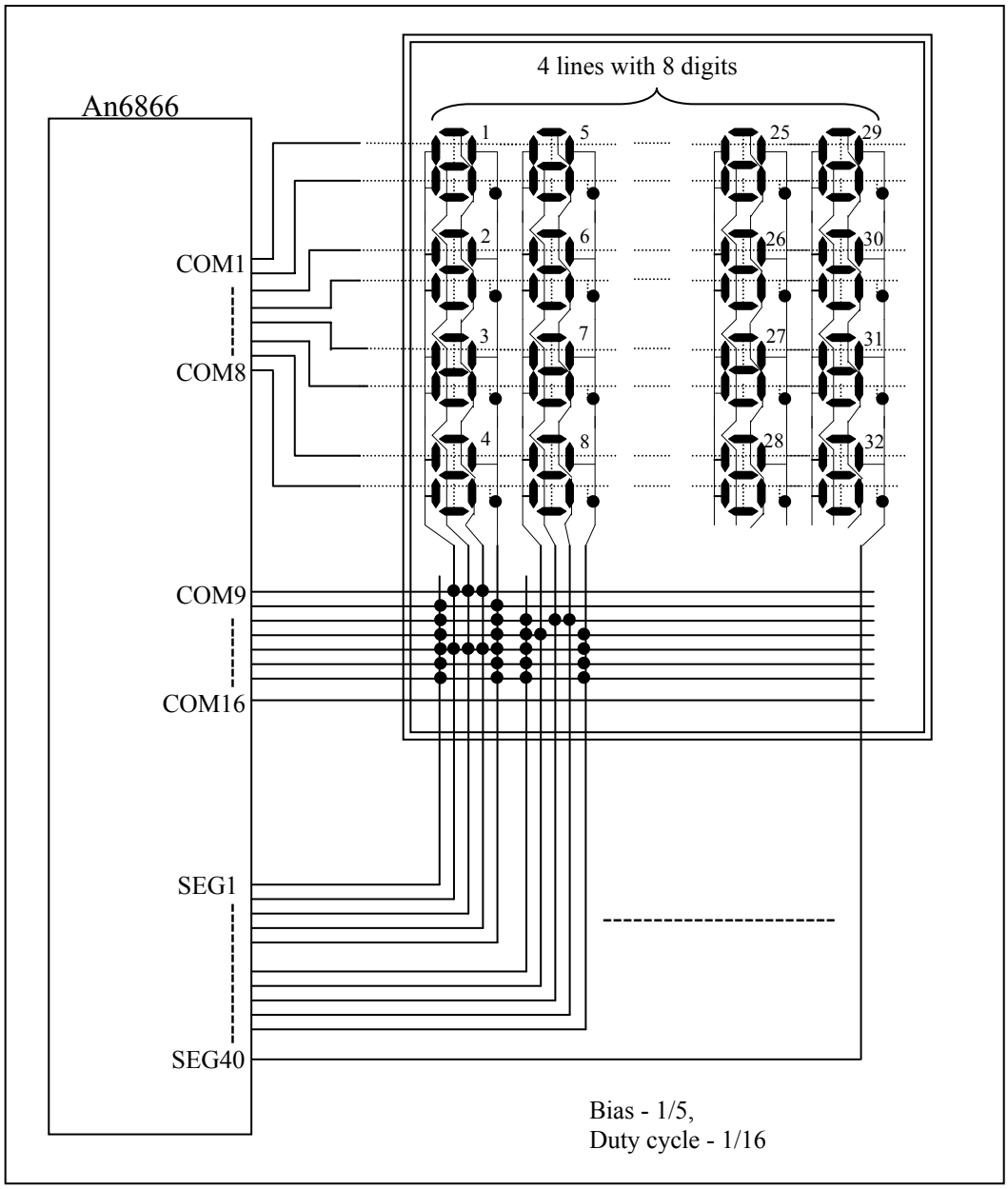


Figure 30. Example of 32 7-segment digits and 8-character dot matrix display.

APPENDIX 1

An6866 Order Form for Standard and Extended Modes

Function	Standard Mode XMODE=1	Extended Mode XMODE=0	Comments
1. Standard CGROM mask option	☐		This parameter is specified only when one of the standard CGROM mask options is selected. When the customer's own code is ordered a respective form is to be attached hereto, then this parameter is omitted (dash instead).
2. Two CGROM pages selection	☐ – yes ☐ – 1st page ☐ – 2nd page	☐ – yes ☐ – 1st page ☐ – 2nd page	If "yes" then software selection of two CGROM pages is enabled for appropriate mode. If "1st page" or "2nd page" then only this page is selected for appropriate mode. In this case the hardware page selection by XMODE is expected.
3. Starting address of 2nd CGROM page 4. Final address of 2nd CGROM page	☐ ☐		The starting and final addresses of 2nd CGROM page are set when selection of two CGROM pages (i.2) is enabled at least in one of the modes. The addresses of table columns are specified either in hex, or decimal or binary form (suffixes h, d, or b respectively). Example: 0E h, 14 d, 1110 b
5. Display Inverse enable	☐ – yes ☐ – no ☐ – fixed	☐ – yes ☐ – no ☐ – fixed	Enabling of program control for display inversion or setting of fixed inversion mode.
6. CGROM characters for 08h-0Fh codes	☐ – yes ☐ – no	☐ – yes ☐ – no	Selection of CGROM characters to 08h-0Fh addresses. It allows to increase number of CGROM characters up to 248. Can be set for each mode separately.
7. Cursor blink enable	☐ – yes ☐ – no	☐ – yes ☐ – no	Setting of blinking cursor with Cursor On and Blink On simultaneously.
8. COM & SEG waveform type	☐ – A-type ☐ – B-type	☐ – A-type ☐ – B-type	Setting of display control at COM & SEG outputs: change of voltage polarity in each COM-line cycle (type A) or in the whole display refresh cycle (type B).
9. Function Set bits state: - Interface data length	☐ – 4 bits (Power On Reset) ☐ – 8 bits (Power On Reset) ☐ – 4 bits (Fixed) ☐ – 8 bits (Fixed)		Selection of initial state of basic mode parameters or their fixing in a definite state (without program control). The parameter can be fixed when the alternative state for this configuration is not required. For example, if 5x11 dot format is coded in CGROM, only this font size and number of lines can be fixed as no other size is available. These parameters can be set for both modes simultaneously.
- Number of display lines	☐ – 1 line (Power On Reset) ☐ – 2 lines (Power On Reset) ☐ – 1 line (Fixed) ☐ – 2 lines (Fixed)		
- Font size	☐ – 5x8 (Power On Reset) ☐ – 5x8 (Fixed) ☐ – 5x11 (Fixed)		
10. On-chip V_{LCD} bias divider resistors	☐ – No ☐ – 1.7 kΩ ☐ – 3 kΩ	☐ – 1.5 kΩ ☐ – 2 kΩ ☐ – 4 kΩ	Presence and nominal value of on-chip V_{LCD} divider resistors
11. On-chip clock oscillator resistor	☐ – No Nominal value at ☐ – Vdd=5V	☐ – Vdd=3V	Presence of on-chip clock oscillator resistor and a frequency setting option

Customer _____ / /

"___" _____ 200_ .

APPENDIX 2

CGROM Pattern Form for Standard and Extended Modes (for An6866)

1st CGROM page (font 5x8 and 5x11)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	(0)															
1	(1)															
2	(2)															
3	(3)															
4	(4)															
5	(5)															
6	(6)															
7	(7)															
8																
9																
A																
B																
C																
D																
E																
F																

Customer _____ / ..... /
"___" _____ **200_ .**

CGROM Pattern Form for Standard and Extended Modes (for An6866)

2nd CGROM page (font 5x8)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	(0)															
1	(1)															
2	(2)															
3	(3)															
4	(4)															
5	(5)															
6	(6)															
7	(7)															
8																
9																
A																
B																
C																
D																
E																
F																

Customer _____ / ..... /

"___" _____ 200_

APPENDIX 3

Released CGROM Patterns

S00 pattern. 2nd page start address 1h
2nd page end address ..... Dh
using 08h-0Fh code range for CGROM..... no

Page 1

S00 pattern

Page 2 **Characters in E, F columns are selected from 1st page**

Lower 4-bit (D0 to D3) of Character Code (hex.)	Higher 4-bit (D4 to D7) of Character Code (hex.)																
		Ø	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Ø	CG RAM (1)	±		Ø	@	P	'	p	ら	é	á	'	ſ	M	X	X	
1	CG RAM (2)	≡	!	1	A	Q	a	q	ü	æ	í	¨	J	†	X	X	
2	CG RAM (3)		"	2	B	R	b	r	é	Æ	ó	°	∞	ş	X	X	
3	CG RAM (4)		#	3	C	S	c	s	ä	ô	ú	'	▷	¶	X	X	
4	CG RAM (5)		$	4	D	T	d	t	à	ö	¢	'	↵	Γ	X	X	
5	CG RAM (6)		%	5	E	U	e	u	à	ò	£	½	↑	⊿	X	X	
6	CG RAM (7)		&	6	F	V	f	v	à	û	¥	¼	↓	Θ	X	X	
7	CG RAM (8)		'	7	G	W	g	w	ら	ù	R	×	→	Λ	X	X	
8	CG RAM (1)		(	8	H	X	h	x	ê	ÿ	ƒ	÷	←	Ξ	X	X	
9	CG RAM (2)		)	9	I	Y	i	y	ë	Ö	¡	≤	Γ	Π	X	X	
A	CG RAM (3)	≈	*	:	J	Z	j	z	è	Ü	ª	≥	¬	Σ	X	X	
B	CG RAM (4)		+	;	K	[	k	{	ï	ñ	º	«	L	↑	X	X	
C	CG RAM (5)	=	,	<	L	\	l	|	î	Ñ	ø	»	⌟	Φ	X	X	
D	CG RAM (6)	∿	−	=	M	]	m	}	ì	ª	ø	≠	·	Ψ	X	X	
E	CG RAM (7)	²	.	>	N	^	n	~	Ä	Ø	ø	√	Θ	Ω	X	X	
F	CG RAM (8)	³	/	?	O	_	o	△	Å	¿	φ	¯	Θ	α	X	X	

S01 pattern. 2nd page start address 2h
2nd page end address ..... Dh
using 08h-0Fh code range for CGROM..... no

Page 1

Lower 4-bit (D0 to D3) of Character Code (hex.)	Higher 4-bit (D4 to D7) of Character Code (hex.)															
	Ø	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Ø	CG RAM (1)															
1	CG RAM (2)															
2	CG RAM (3)															
3	CG RAM (4)															
4	CG RAM (5)															
5	CG RAM (6)															
6	CG RAM (7)															
7	CG RAM (8)															
8	CG RAM (1)															
9	CG RAM (2)															
A	CG RAM (3)															
B	CG RAM (4)															
C	CG RAM (5)															
D	CG RAM (6)															
E	CG RAM (7)															
F	CG RAM (8)															

S01 pattern

Page 2 **Characters in E, F columns are selected from 1st page**

S02 pattern. 2nd page start address 1h
2nd page end address ..... Fh
using 08h-0Fh code range for CGROM..... no

Page 1

Lower 4-bit (D0 to D3) of Character Code (hex.)	Higher 4-bit (D4 to D7) of Character Code (hex.)															
	Ø	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Ø	CG RAM (1)	◇		Ø	@	P	á	p	€	Ĺ	Ł	Ą	À	Đ	à	ą
1	CG RAM (2)	✚	!	1	A	Q	a	q	ŕ	ľ	¡	É	Á	Ń	á	ń
2	CG RAM (3)	◀	"	2	B	R	b	r	Ř	¡	¢	Ă	Â	Ò	â	ò
3	CG RAM (4)	▶	#	3	C	S	c	s	ğ	Ĥ	£	Ö	Ă	Ó	ă	ó
4	CG RAM (5)	■	$	4	D	T	d	t	„	í	J	ó	Ä	ô	ä	ô
5	CG RAM (6)	Я	%	5	E	U	e	u	…	●	¤	ć	Å	ő	å	ő
6	CG RAM (7)	Ю	&	6	F	V	f	v	Б	ý	ĵ	č	Ę	Ö	ę	ö
7	CG RAM (8)	Э	'	7	G	W	g	w	Г	–	ď	·	Ç	ï	÷	Δ
8	CG RAM (1)	Ь	(	8	H	X	h	x	Д	Ж	Ů	Ę	È	Ø	è	ø
9	CG RAM (2)	Ы	)	9	I	Y	i	y	ś	ş	Ű	Ě	é	Ù	é	ù
A	CG RAM (3)	Ъ	*	:	J	Z	j	z	š	ş	ə	Ō	Ê	Ú	ê	ú
B	CG RAM (4)	Ш	+	;	K	[	k	ǯ	θ	Σ	«	»	Ë	Û	ë	û
C	CG RAM (5)	Щ	,	<	L	\	l	|	€	œ	Ǯ	Ń	ì	Ü	ì	ü
D	CG RAM (6)	Ч	-	=	M	]	m	И	Й	Л	Ψ	Ň	í	Ý	í	ý
E	CG RAM (7)	Ц	.	>	N	^	n	П	ž	ż	ź	ż	î	Þ	î	þ
F	CG RAM (8)	ф	/	?	O	_	o	Ť	У	Ÿ	Ω	¿	ï	ß	ï	ÿ

S02 pattern

Page 2

S03 pattern. 2nd page start address 0h
2nd page end address ..... Fh
using 08h-0Fh code range for CGROM..... yes

Page 1

Lower 4-bit (D0 to D3) of Character Code (hex.)	Higher 4-bit (D4 to D7) of Character Code (hex.)															
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	CG RAM (1)															
1	CG RAM (2)															
2	CG RAM (3)															
3	CG RAM (4)															
4	CG RAM (5)															
5	CG RAM (6)															
6	CG RAM (7)															
7	CG RAM (8)															
8																
9																
A																
B																
C																
D																
E																
F																

S03 pattern

Page 2

S06 pattern. 2nd page start address 1h
2nd page end address ..... Fh
using 08h-0Fh code range for CGROM..... no

Page 1

Lower 4-bit (D0 to D3) of Character Code (hex.)	Higher 4-bit (D4 to D7) of Character Code (hex.)																
		Ø	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Ø	CG RAM (1)																
1	CG RAM (2)																
2	CG RAM (3)																
3	CG RAM (4)																
4	CG RAM (5)																
5	CG RAM (6)																
6	CG RAM (7)																
7	CG RAM (8)																
8	CG RAM (1)																
9	CG RAM (2)																
A	CG RAM (3)																
B	CG RAM (4)																
C	CG RAM (5)																
D	CG RAM (6)																
E	CG RAM (7)																
F	CG RAM (8)																

S06 pattern

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APPENDIX 4

Released Mask Options of An6866

An6866-0000

Parameter	Standard Mode XMODE=1	Extended Mode XMODE=0
1. CGROM pattern	S00	
2. CGROM page	1st page	Software controlled (P bit of Function Set instruction)
5. Display inversion enabling	no	Software controlled (I bit of Function Set instruction)
7. Underline cursor blinking enable	no	yes
8. Display Waveform type	A-type	B-type
9. Function Set: - Interface data bus width - Number of display lines - Font size	 8 bit (init) 1 line (init) 5x8 (init)	
10. On-chip V_{LCD} divider resistors	No	
11. On-chip oscillator resistor	No	

Address		Identification Code of An6866-0000								Parameter
Dec.	Hex.	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Value
120	78	0	1	0	0	0	0	0	1	41	Chip Identifier
121	79	0	1	0	0	1	1	1	0	4E	
122	7A	0	1	0	0	0	1	0	0	44	
123	7B	0	1	0	0	0	0	1	0	42	
124	7C	0	0	0	0	0	0	0	0	00	CGROM version
125	7D	0	0	0	0	0	1	0	1	05	Configuration
126	7E	0	0	0	1	0	1	P	I	*	Config./Current state
127	7F	X	N	F	D	C	B	ID	SH	*	Current state

An6866-0100

Parameter	Standard Mode XMODE=1	Extended Mode XMODE=0
1. CGROM pattern	S00	
2. CGROM page	1st page	2nd page
5. Display inversion enabling	no	no
7. Underline cursor blinking enable	no	yes
8. Display Waveform type	A-type	B-type
9. Function Set: - Interface data bus width - Number of display lines - Font size	 8 bit (init) 1 line (init) 5x8 (init)	
10. On-chip V_{LCD} divider resistors	No	
11. On-chip oscillator resistor	No	

Address		Identification Code of An6866-0100									Parameter
Dec.	Hex.	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Value (hex)	
120	78	0	1	0	0	0	0	0	1	41	Chip Identifier
121	79	0	1	0	0	1	1	1	0	4E	
122	7A	0	1	0	0	0	1	0	0	44	
123	7B	0	1	0	0	0	0	1	0	42	
124	7C	1	0	0	0	0	0	0	0	80	CGROM version
125	7D	0	0	0	0	0	1	0	0	04	Configuration
126	7E	0	0	0	1	0	1	P	I	*	Config./Current state
127	7F	X	N	F	D	C	B	ID	SH	*	Current state

An6866-0101

Parameter	Standard Mode XMODE=1	Extended Mode XMODE=0
1. CGROM pattern	S01	
2. CGROM page	1st page	2nd page
5. Display inversion enabling	no	no
7. Underline cursor blinking enable	no	yes
8. Display Waveform type	A-type	B-type
9. Function Set: - Interface data bus width - Number of display lines - Font size	 8 bit (init) 1 line (init) 5x8 (init)	
10. On-chip V_{LCD} divider resistors	No	
11. On-chip oscillator resistor	No	

Address		Identification Code of An6866-0101									Parameter
Dec.	Hex.	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Value (hex)	
120	78	0	1	0	0	0	0	0	1	41	Chip Identifier
121	79	0	1	0	0	1	1	1	0	4E	
122	7A	0	1	0	0	0	1	0	0	44	
123	7B	0	1	0	0	0	0	1	0	42	
124	7C	1	0	0	0	0	0	0	1	81	CGROM version
125	7D	0	0	0	0	0	1	0	0	04	Configuration
126	7E	0	0	0	1	0	1	P	I	*	Config./Current state
127	7F	X	N	F	D	C	B	ID	SH	*	Current state

An6866-0200

Parameter	Standard Mode XMODE=1	Extended Mode XMODE=0
1. CGROM pattern	S00	
2. CGROM page	1st page	2nd page
5. Display inversion enabling	no	no
7. Underline cursor blinking enable	no	yes
8. Display Waveform type	B-type	B-type
9. Function Set: - Interface data bus width - Number of display lines - Font size	 8 bit (init) 1 line (init) 5x8 (init)	
10. On-chip V_{LCD} divider resistors	No	
11. On-chip oscillator resistor	No	

Address		Identification Code of An6866-0200									Parameter
Dec.	Hex.	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Value (hex)	
120	78	0	1	0	0	0	0	0	1	41	Chip Identifier
121	79	0	1	0	0	1	1	1	0	4E	
122	7A	0	1	0	0	0	1	0	0	44	
123	7B	0	1	0	0	0	0	1	0	42	
124	7C	1	0	0	0	0	0	0	0	80	CGROM version
125	7D	0	0	0	0	0	1	0	0	04	Configuration
126	7E	0	0	0	1	1	1	P	I	*	Config./Current state
127	7F	X	N	F	D	C	B	ID	SH	*	Current state

An6866-0201

Parameter	Standard Mode XMODE=1	Extended Mode XMODE=0
1. CGROM pattern	S01	
2. CGROM page	1st page	2nd page
5. Display inversion enabling	no	no
7. Underline cursor blinking enable	no	yes
8. Display Waveform type	B-type	B-type
9. Function Set: - Interface data bus width - Number of display lines - Font size	 8 bit (init) 1 line (init) 5x8 (init)	
10. On-chip V_{LCD} divider resistors	No	
11. On-chip oscillator resistor	No	

Address		Identification Code of An6866-0201									Parameter
Dec.	Hex.	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Value (hex)	
120	78	0	1	0	0	0	0	0	1	41	Chip Identifier
121	79	0	1	0	0	1	1	1	0	4E	
122	7A	0	1	0	0	0	1	0	0	44	
123	7B	0	1	0	0	0	0	1	0	42	
124	7C	1	0	0	0	0	0	0	1	81	CGROM version
125	7D	0	0	0	0	0	1	0	0	04	Configuration
126	7E	0	0	0	1	1	1	P	I	*	Config./Current state
127	7F	X	N	F	D	C	B	ID	SH	*	Current state

An6866-0202

Parameter	Standard Mode XMODE=1	Extended Mode XMODE=0
1. CGROM pattern	S02	
2. CGROM page	1st page	2nd page
5. Display inversion enabling	no	no
7. Underline cursor blinking enable	no	no
8. Display Waveform type	B-type	B-type
9. Function Set: - Interface data bus width - Number of display lines - Font size	 8 bit (init) 1 line (init) 5x8 (init)	
10. On-chip V_{LCD} divider resistors	No	
11. On-chip oscillator resistor	No	

Address		Identification Code of An6866-0202									Parameter
Dec.	Hex.	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Value (hex)	
120	78	0	1	0	0	0	0	0	1	41	Chip Identifier
121	79	0	1	0	0	1	1	1	0	4E	
122	7A	0	1	0	0	0	1	0	0	44	
123	7B	0	1	0	0	0	0	1	0	42	
124	7C	1	0	0	0	0	0	1	0	82	CGROM version
125	7D	0	0	0	0	0	1	0	0	04	Configuration
126	7E	0	0	0	0	1	1	P	I	*	Config./Current state
127	7F	X	N	F	D	C	B	ID	SH	*	Current state

An6866-0306

Parameter	Standard Mode XMODE=1	Extended Mode XMODE=0
1. CGROM pattern	S06	
2. CGROM page	1st page	2nd page
5. Display inversion enabling	no	no
7. Underline cursor blinking enable	no	yes
8. Display Waveform type	B-type	B-type
9. Function Set: - Interface data bus width - Number of display lines - Font size	 8 bit (init) 1 line (init) 5x8 (init)	
10. On-chip V_{LCD} divider resistors	2kΩ	
11. On-chip oscillator resistor	Nominal clock frequency at V_{DD}=3V	

Address		Identification Code of An6866-0306									Parameter
Dec.	Hex.	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Value (hex)	
120	78	0	1	0	0	0	0	0	1	41	Chip Identifier
121	79	0	1	0	0	1	1	1	0	4E	
122	7A	0	1	0	0	0	1	0	1	45	
123	7B	0	1	0	0	0	0	1	0	42	
124	7C	1	0	0	0	0	1	1	0	86	CGROM version
125	7D	0	0	0	0	0	1	0	0	04	Configuration
126	7E	0	0	0	1	1	1	P	I	*	Config./Current state
127	7F	X	N	F	D	C	B	ID	SH	*	Current state

An6866-0403

Parameter	Standard Mode XMODE=1	Extended Mode XMODE=0
1. CGROM pattern	S03	
2. CGROM page	1st page	Software controlled (P bit of Function Set instruction)
5. Display inversion enabling	no	no
7. Underline cursor blinking enable	yes	yes
8. Display Waveform type	B-type	B-type
9. Function Set: - Interface data bus width - Number of display lines - Font size	 8 bit (init) 2 line (init) 5x8 (fix)	
10. On-chip V_{LCD} divider resistors	2kΩ	
11. On-chip oscillator resistor	Nominal clock frequency at V_{DD}=5V	

Address		Identification Code of An6866-0403									Parameter
Dec.	Hex.	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Value (hex)	
120	78	0	1	0	0	0	0	0	1	41	Chip Identifier
121	79	0	1	0	0	1	1	1	0	4E	
122	7A	0	1	0	0	0	1	1	0	46	
123	7B	0	1	0	0	0	0	1	0	42	
124	7C	0	0	0	0	0	0	1	1	03	CGROM version
125	7D	1	0	0	1	0	1	0	0	94	Configuration
126	7E	0	0	1	1	1	1	P	I	*	Config./Current state
127	7F	X	N	F	D	C	B	ID	SH	*	Current state

Mask Option Selection

Mask Option	An6866-0000		An6866-0100		An6866-0101		An6866-0200	
Mode	Standard Mode XMODE=1	Extended Mode XMODE=0	Standard Mode XMODE=1	Extended Mode XMODE=0	Standard Mode XMODE=1	Extended Mode XMODE=0	Standard Mode XMODE=1	Extended Mode XMODE=0
CGROM pattern	S00		S00		S01		S00	
CGROM page (fix page number or "P" - software control)	1	P	1	2	1	2	1	2
Display inversion enabling ("0" - no, "1" - yes)	0	1	0	0	0	0	0	0
Underline cursor blinking enable ("0" -no, "1" - yes)	0	1	0	1	0	1	0	1
Display Waveform type	A	B	A	B	A	B	B	B
Function Set:								
- Interface data bus width (DL: "0" - 4 bit., "1" - 8 bit.)	1 (init)		1 (init)		1 (init)		1 (init)	
- Number of display lines (N: "0" - 1 line, "1" - 2 lines)	0 (init)		0 (init)		0 (init)		0 (init)	
- Font size (F: "0" - 5x8 font, "1" - 5x11 font)	0 (init)		0 (init)		0 (init)		0 (init)	
On-chip V_{LCD} divider resistors	-		-		-		-	
On-chip oscillator resistor	-		-		-		-	

Mask Option Selection (continue)

Mask Option	An6866-0201		An6866-0202		An6866-0306		An6866-0403	
Mode	Standard Mode XMODE=1	Extended Mode XMODE=0	Standard Mode XMODE=1	Extended Mode XMODE=0	Standard Mode XMODE=1	Extended Mode XMODE=0	Standard Mode XMODE=1	Extended Mode XMODE=0
CGROM pattern	S01		S02		S03		S06	
CGROM page (fix page number or "P" - software control)	1	2	1	2	1	2	1	P
Display inversion enabling ("0" - no, "1" - yes)	0	0	0	0	0	0	0	0
Underline cursor blinking enable ("0" -no, "1" - yes)	0	1	0	0	0	1	1	1
Display Waveform type	B	B	B	B	B	B	B	B
Function Set:								
- Interface data bus width (DL: "0" - 4 bit., "1" - 8 bit.)	1 (init)		1 (init)		1 (init)		1 (init)	
- Number of display lines (N: "0" - 1 line, "1" - 2 lines)	0 (init)		0 (init)		0 (init)		1 (init)	
- Font size (F: "0" - 5x8 font, "1" - 5x11 font)	0 (init)		0 (init)		0 (init)		0 (fix)	
On-chip V_{LCD} divider resistors	-		-		2kΩ		3kΩ	
On-chip oscillator resistor	-		-		Fnom at V_{DD}=3V		Fnom at V_{DD}=5V	