

## 6.2A, 600V, 1.200 Ohm, N-Channel Power MOSFET

This N-Channel enhancement mode silicon gate power field effect transistor is an advanced power MOSFET designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching convertors, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

Formerly developmental type TA17426.

## Ordering Information

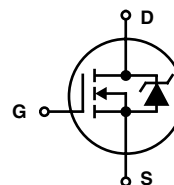
PART NUMBER	PACKAGE	BRAND
IRFBC40	TO-220AB	IRFBC40

NOTE: When ordering, include the entire part number.

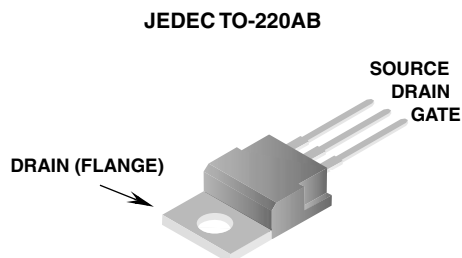
## Features

- 6.2A, 600V
- $r_{DS(ON)} = 1.200\Omega$
- Single Pulse Avalanche Energy Rated
- Simple Drive Requirements
- Ease of Paralleling
- Related Literature
  - TB334, "Guidelines for Soldering Surface Mount Components to PC Boards"

## Symbol



## Packaging



# IRFBC40

## Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

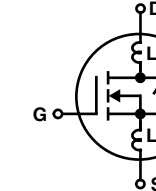
	IRFBC40	UNITS
Drain to Source Breakdown Voltage (Note 1) . . . . .	$V_{DS}$ 600	V
Drain to Gate Voltage ( $R_{GS} = 20\text{k}\Omega$ ) (Note 1) . . . . .	$V_{DGR}$ 600	V
Continuous Drain Current . . . . .	$I_D$ 6.2	A
$T_C = 100^\circ\text{C}$ . . . . .	$I_D$ 3.9	A
Pulsed Drain Current (Note 2) . . . . .	$I_{DM}$ 25	A
Gate to Source Voltage . . . . .	$V_{GS}$ $\pm 20$	V
Maximum Power Dissipation . . . . .	$P_D$ 125	W
Linear Derating Factor . . . . .	1.0	$\text{W}/^\circ\text{C}$
Single Pulse Avalanche Energy Rating (Note 2) (See Figures 15,16). . . . .	$E_{AS}$ 570	mJ
Operating and Storage Temperature . . . . .	$T_J, T_{STG}$ -55 to 150	$^\circ\text{C}$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s. . . . .	$T_L$ 300	$^\circ\text{C}$
Package Body for 10s, See Techbrief 334 . . . . .	$T_{pkg}$ 260	$^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### NOTE:

1.  $T_J = 25^\circ\text{C}$  to  $125^\circ\text{C}$ .

## Electrical Specifications $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA, (Figure 11)		600	-	-	V
Gate to Source Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250μA		2.0	-	4.0	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = Rated BV <sub>DSS</sub> , V <sub>GS</sub> = 0V		-	-	25	μA
		V <sub>DS</sub> = 0.8 x Rated BV <sub>DSS</sub> , V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C		-	-	250	μA
On-State Drain Current (Note 4)	I <sub>D(ON)</sub>	V <sub>DS</sub> > I <sub>D(ON)</sub> x r <sub>DS(ON)MAX</sub> , V <sub>GS</sub> = 10V		6.2	-	-	A
Gate to Source Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ±20V		-	-	±100	nA
Drain to Source On Resistance (Note 2)	r <sub>DS(ON)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 3.4A (Figures 9, 10)		-	0.97	1.2	Ω
Forward Transconductance (Note 4)	g <sub>fs</sub>	V <sub>DS</sub> ≥ 100V, I <sub>DS</sub> = 3.4A (Figure 13)		4.7	70	-	S
Turn-On Delay Time	t <sub>d(ON)</sub>	V <sub>DD</sub> = 300V, I <sub>D</sub> ≈ 6.2A, R <sub>G</sub> = 9.1Ω, V <sub>GS</sub> = 10V, R <sub>L</sub> = 47Ω Switching Speeds are Essentially independent of Operating Temperature		-	13	20	ns
Rise Time	t <sub>r</sub>			-	18	27	ns
Turn-Off Delay Time	t <sub>d(OFF)</sub>			-	55	83	ns
Fall Time	t <sub>f</sub>			-	20	30	ns
Total Gate Charge (Gate to Source + Gate to Drain)	Q <sub>g(TOT)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 6.2A, V <sub>DS</sub> = 0.7 x Rated BV <sub>DSS</sub> (Figure 14) Gate Charge is Essentially Independent of Operating Temperature		-	40	60	nC
Gate to Source Charge	Q <sub>gs</sub>			-	5.5	-	nC
Gate to Drain “Miller” Charge	Q <sub>gd</sub>			-	20	-	nC
Input Capacitance	C <sub>ISS</sub>	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 25V, f = 1.0MHz (Figure 12)		-	1300	-	pF
Output Capacitance	C <sub>OSS</sub>			-	160	-	pF
Reverse Transfer Capacitance	C <sub>RSS</sub>			-	45	-	pF
Internal Drain Inductance	L <sub>D</sub>	Measured from the Drain Lead, 6mm (0.25in) from Package to Center of Die	Modified MOSFET Symbol Showing the Internal Devices Inductances 	-	4.5	-	nH
Internal Source Inductance	L <sub>S</sub>	Measured from the Source Lead, 6mm (0.25in) from Header to Source Bonding Pad		-	7.5	-	nH
Thermal Resistance Junction to Case	R <sub>θJC</sub>			-	-	1.0	°C/W
Thermal Resistance Junction to Ambient	R <sub>θJA</sub>	Typical Socket Mount		-	-	80	°C/W

## Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Continuous Source to Drain Current	$I_{SD}$	Modified MOSFET Symbol Showing the Integral Reverse P-N Junction Diode	-	-	6.2	A
Pulse Source to Drain Current (Note 3)	$I_{SDM}$		-	-	25	A
Diode Source to Drain Voltage (Note 2)	$V_{SD}$	$T_J = 25^\circ\text{C}$ , $I_{SD} = 6.2\text{A}$ , $V_{GS} = 0\text{V}$ (Figure 8)	-	-	1.5	V
Reverse Recovery Time	$t_{rr}$	$T_J = 25^\circ\text{C}$ , $I_{SD} = 6.2\text{A}$ , $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	200	450	940	ns
Reverse Recovery Charge	$Q_{RR}$	$T_J = 25^\circ\text{C}$ , $I_{SD} = 6.2\text{A}$ , $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	1.8	3.8	8.0	$\mu\text{C}$

### NOTES:

- Pulse test: pulse width  $\leq 300\mu\text{s}$ , duty cycle  $\leq 2\%$ .
- Repetitive rating: pulse width limited by Max junction temperature. See Transient Thermal Impedance curve (Figure 3).
- $V_{DD} = 50\text{V}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 16\text{mH}$ ,  $R_G = 25\Omega$ , peak  $I_{AS} = 6.8\text{A}$

## Typical Performance Curves Unless Otherwise Specified

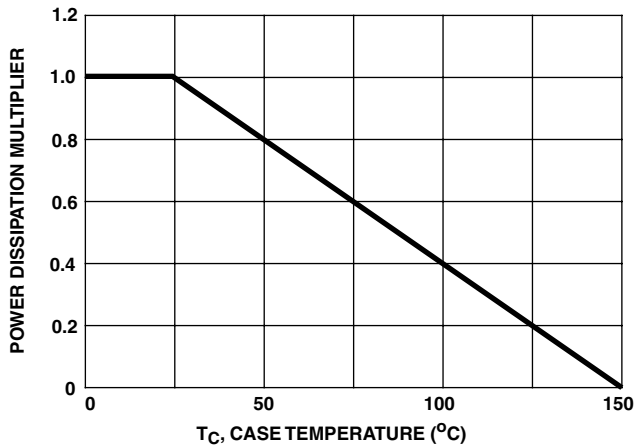


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

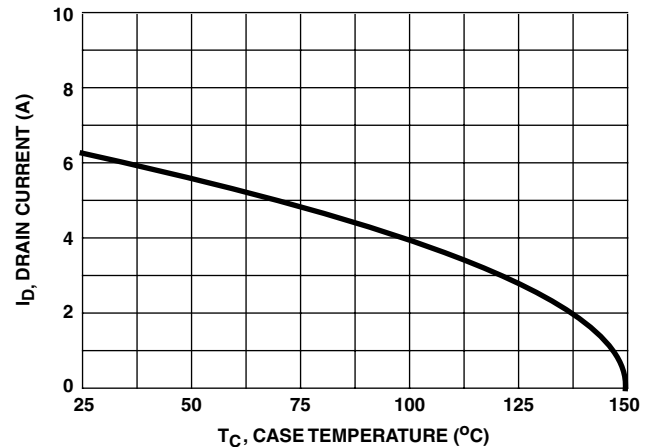


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

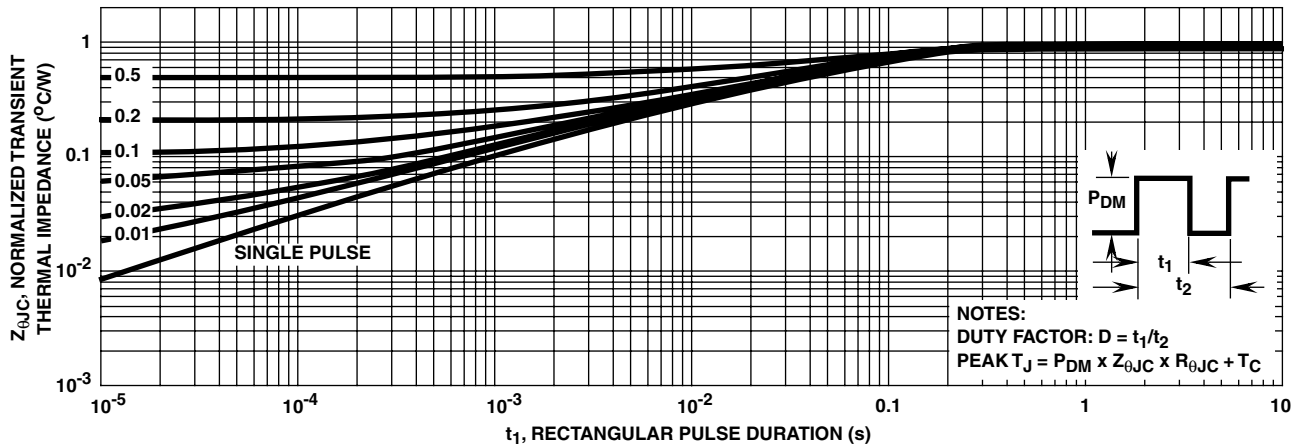


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

**Typical Performance Curves** Unless Otherwise Specified (Continued)

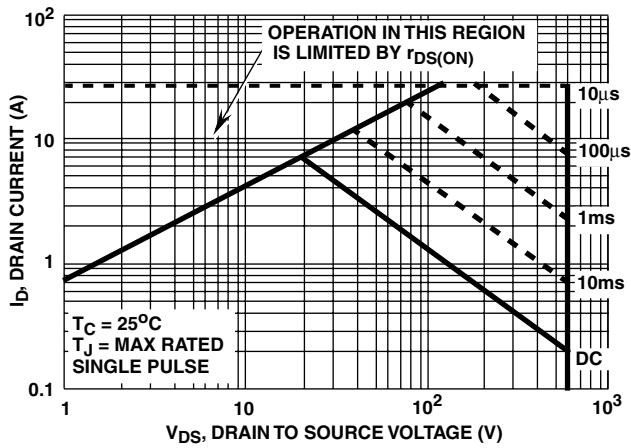


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

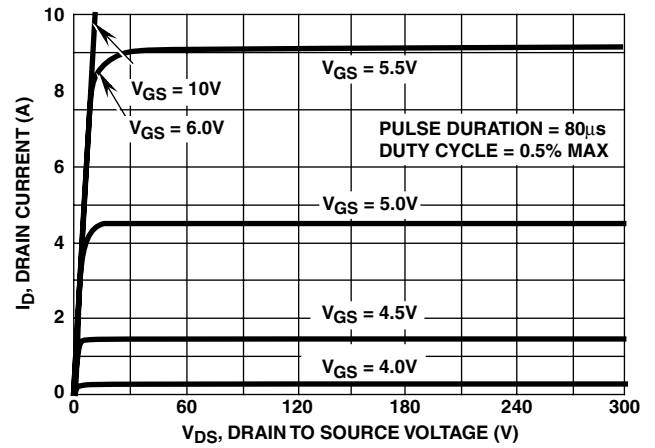


FIGURE 5. OUTPUT CHARACTERISTICS

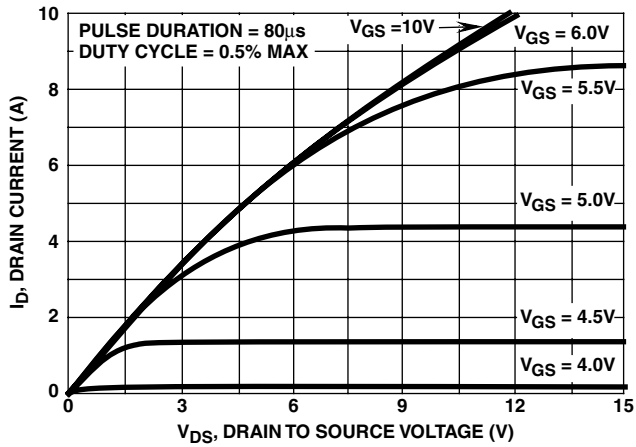


FIGURE 6. SATURATION CHARACTERISTICS

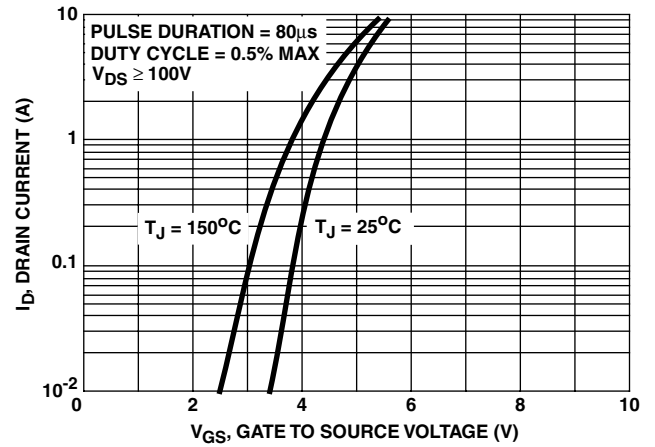


FIGURE 7. TRANSFER CHARACTERISTICS

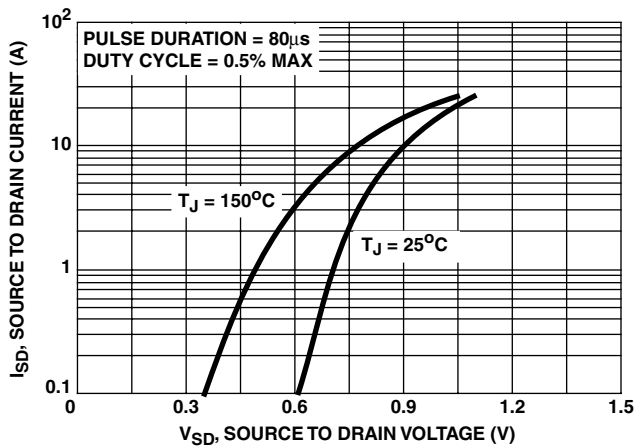


FIGURE 8. SOURCE TO DRAIN DIODE VOLTAGE

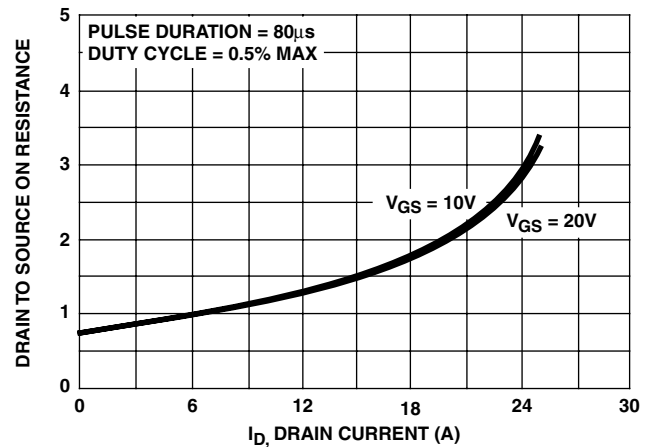


FIGURE 9. DRAIN TO SOURCE ON RESISTANCE vs. GATE VOLTAGE AND DRAIN CURRENT

**Typical Performance Curves** Unless Otherwise Specified (Continued)

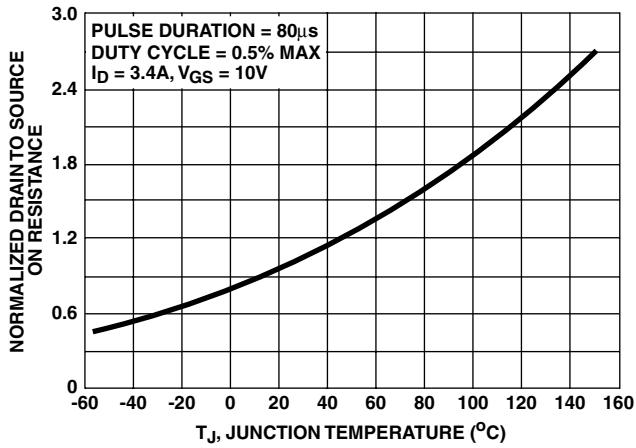


FIGURE 10. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

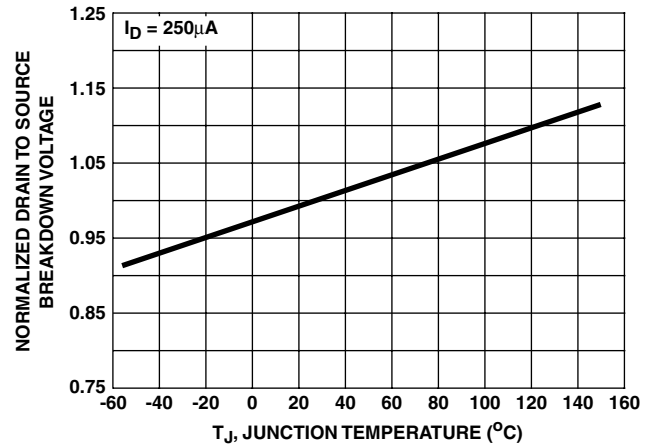


FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

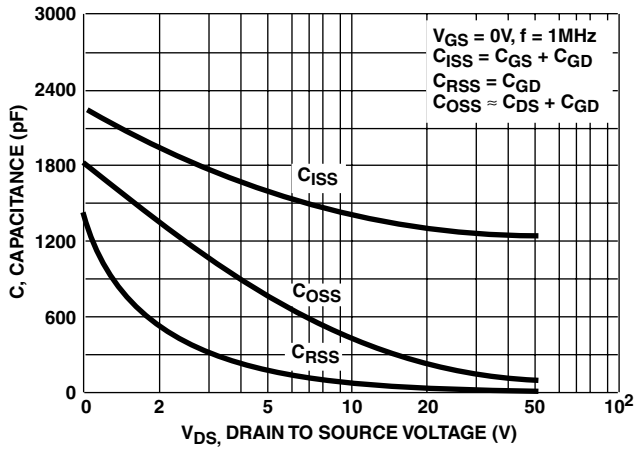


FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

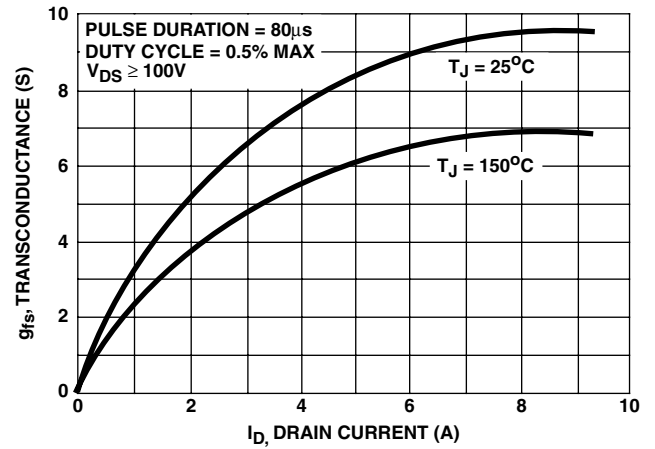


FIGURE 13. TRANSCONDUCTANCE vs DRAIN CURRENT

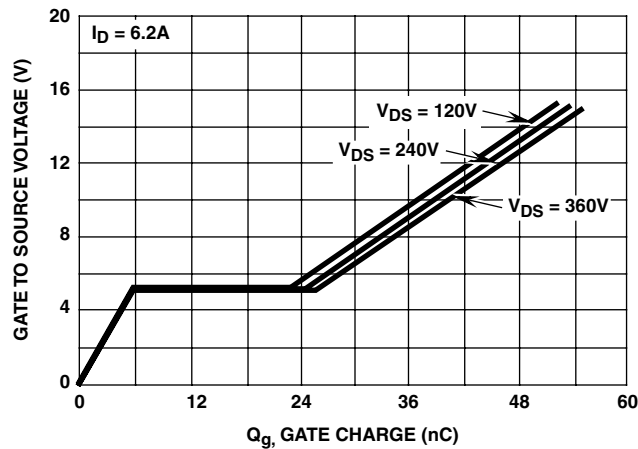


FIGURE 14. GATE TO SOURCE VOLTAGE vs GATE CHARGE

## Test Circuits and Waveforms

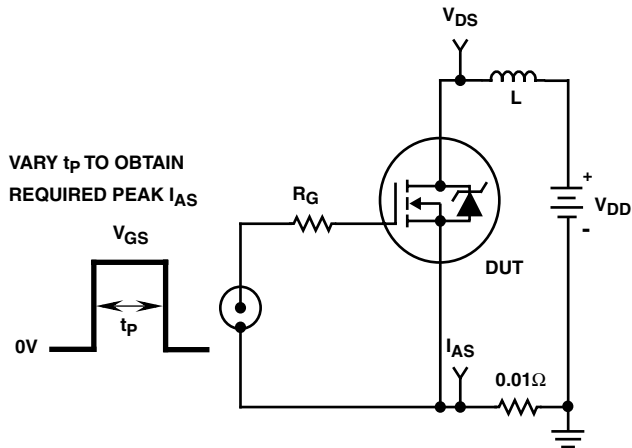


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

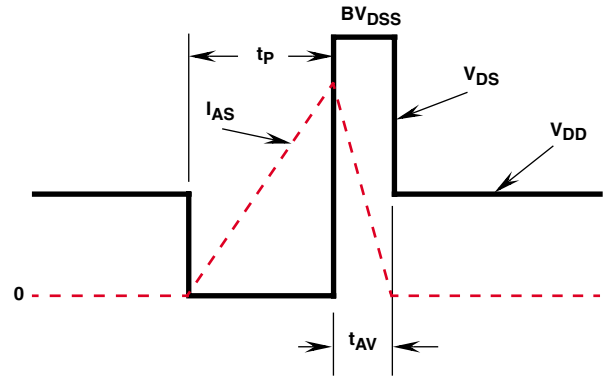


FIGURE 16. UNCLAMPED ENERGY WAVEFORMS

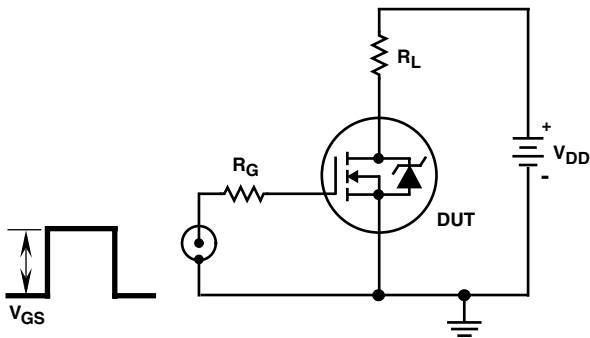


FIGURE 17. SWITCHING TIME TEST CIRCUIT

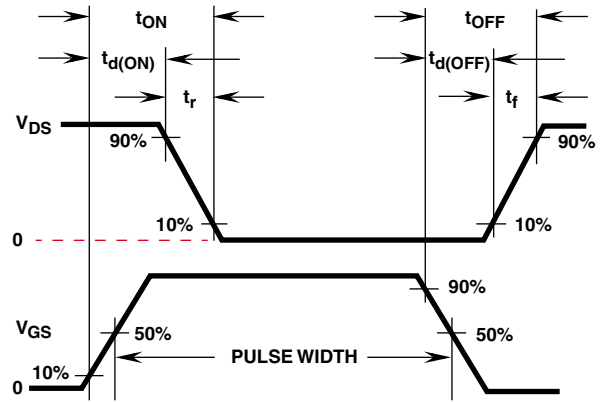


FIGURE 18. RESISTIVE SWITCHING WAVEFORMS

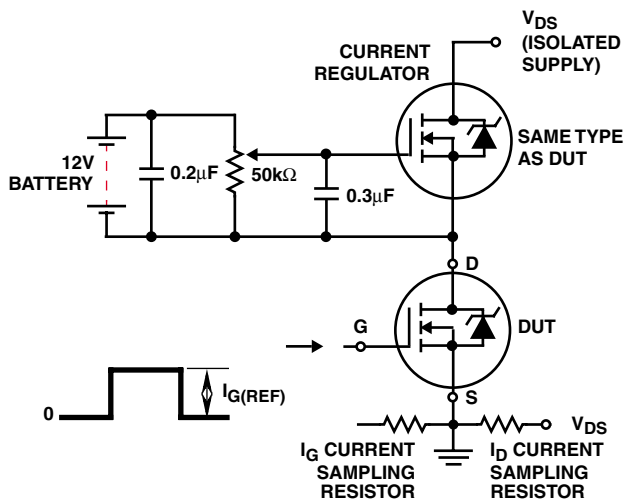


FIGURE 19. GATE CHARGE TEST CIRCUIT

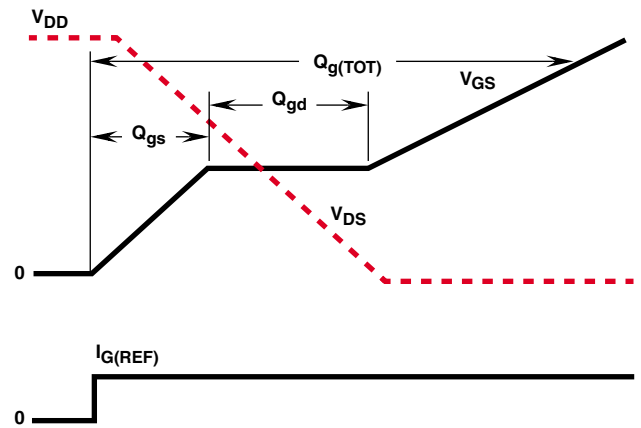


FIGURE 20. GATE CHARGE WAVEFORMS

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